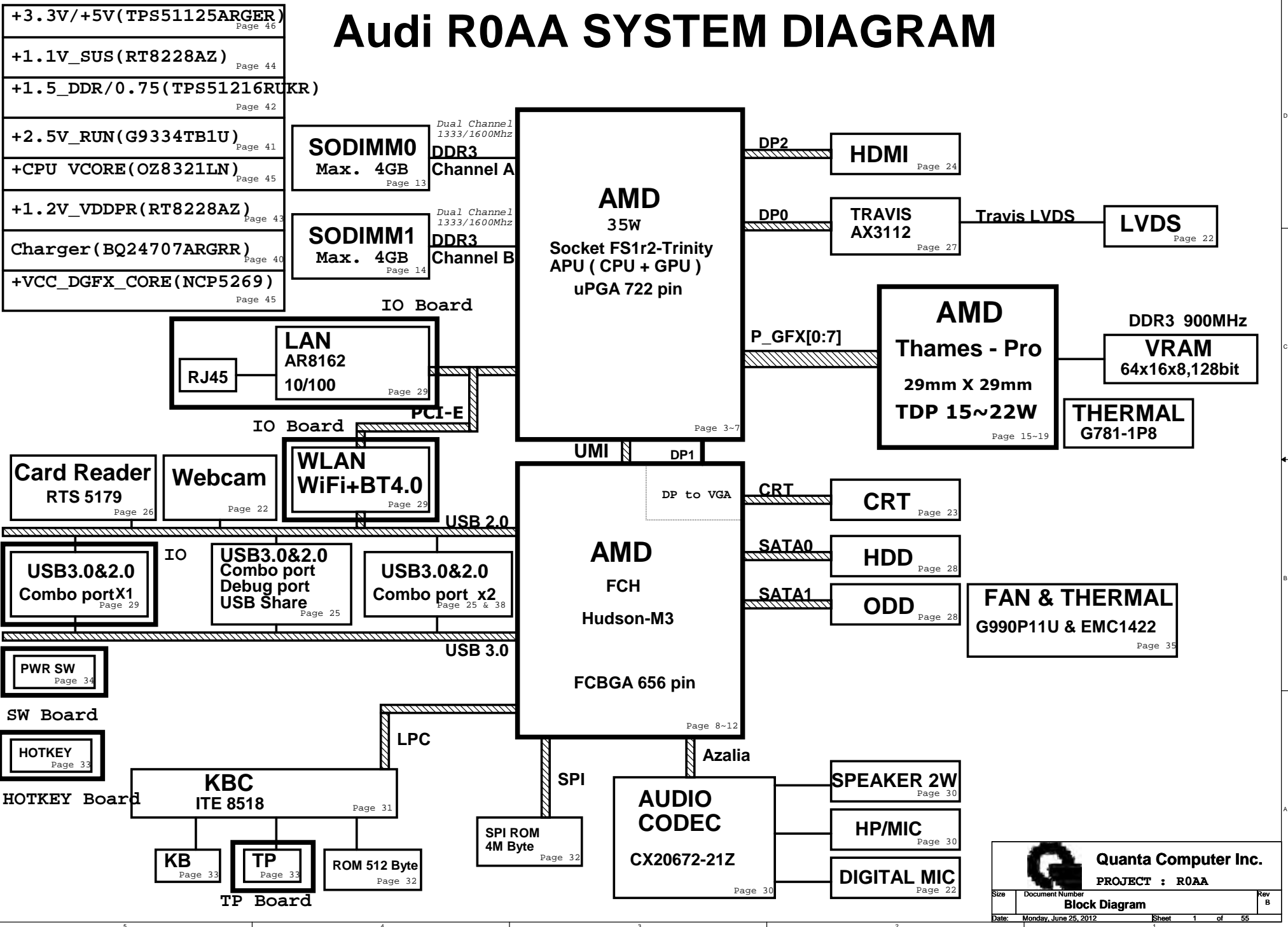


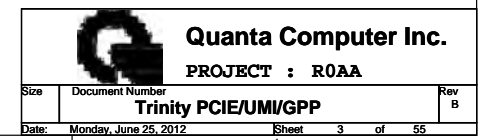
# Audi R0AA SYSTEM DIAGRAM

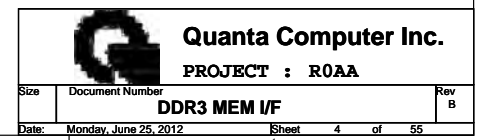


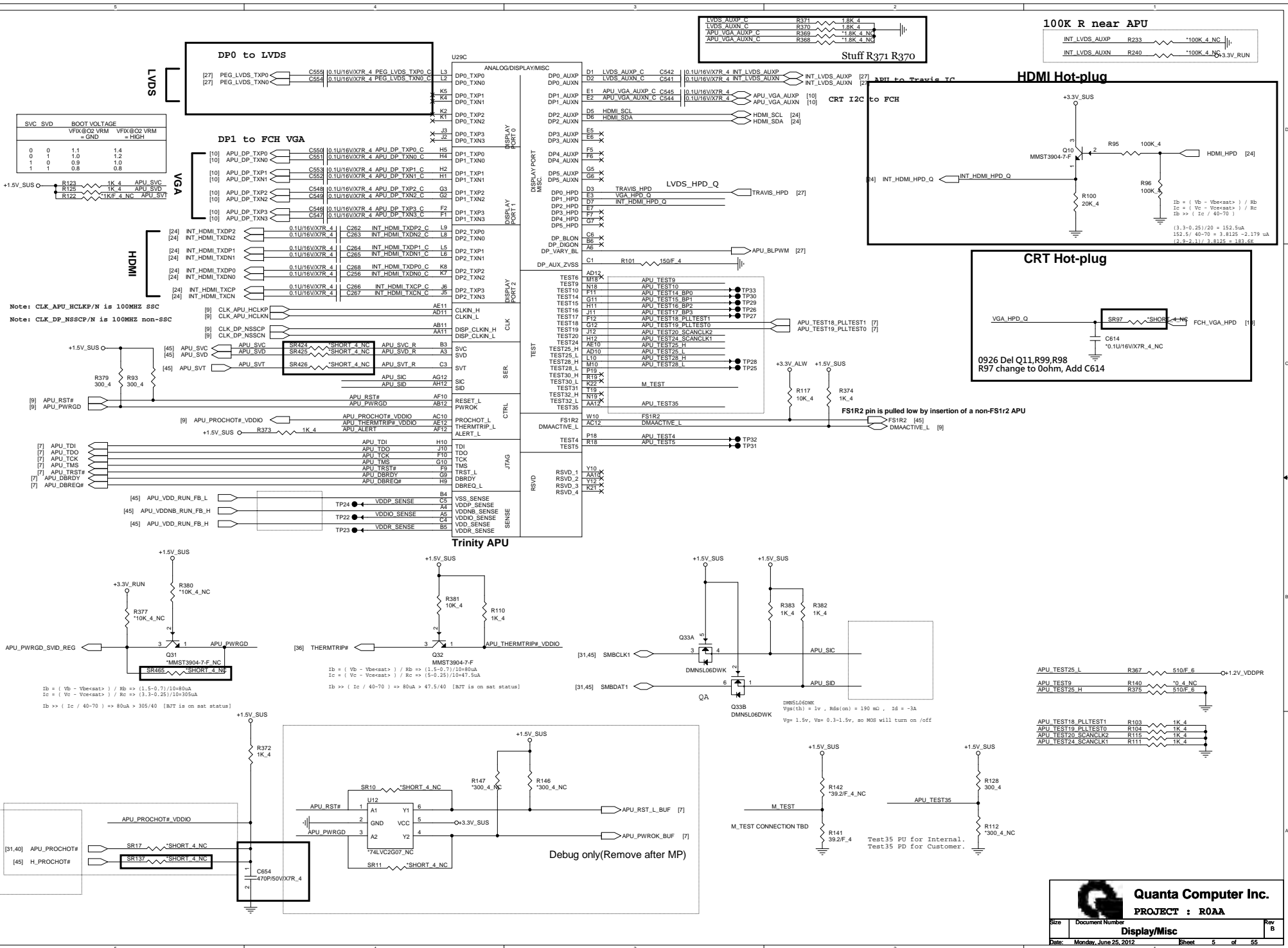
USB Master	Port Assignment
USB0	DEBUG
USB1	MiniCard 1 (WLAN/BT)
USB2	NC
USB3	NC
USB4	NC
USB5	NC
USB6	NC
USB7	Card Reader
USB8	NC
USB9	Camera
USB10	External port#1 (USB3.0)
USB11	External port#2 (USB3.0)
USB12	External port#3 (USB3.0)
USB13	External port#4 (Power share)

SATA Master	Port Assignment
SATA0	HDD
SATA1	ODD
SATA2	NC
SATA3	NC
SATA4	NC
SATA5	NC

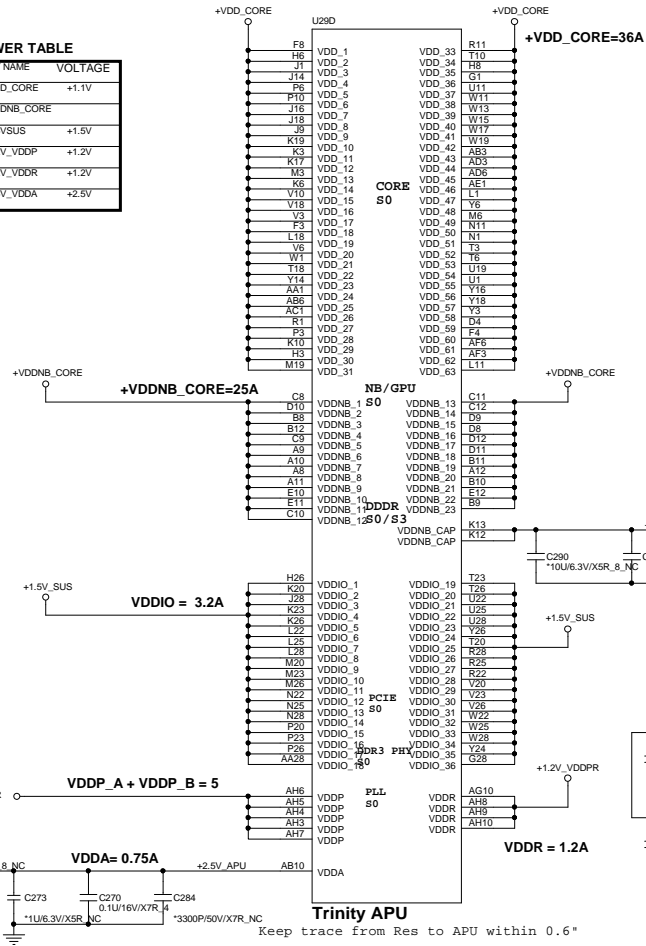
PCIE Master	Port Assignment
CPU_GPP 0	LAN
CPU_GPP 1	WLAN
CPU_GPP 2	NC
CPU_GPP 3	NC
FCH_GPP 0	NC
FCH_GPP 1	NC
FCH_GPP 2	NC
FCH_GPP 3	NC



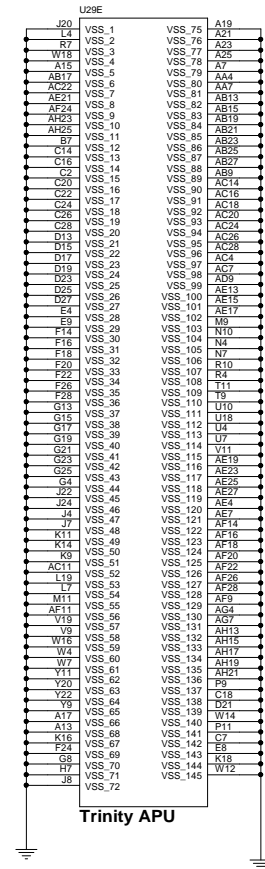
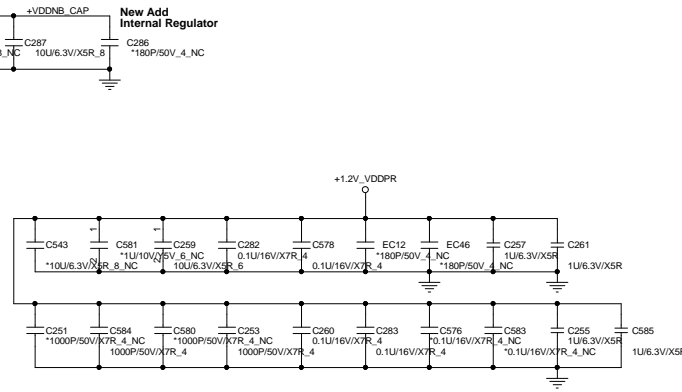




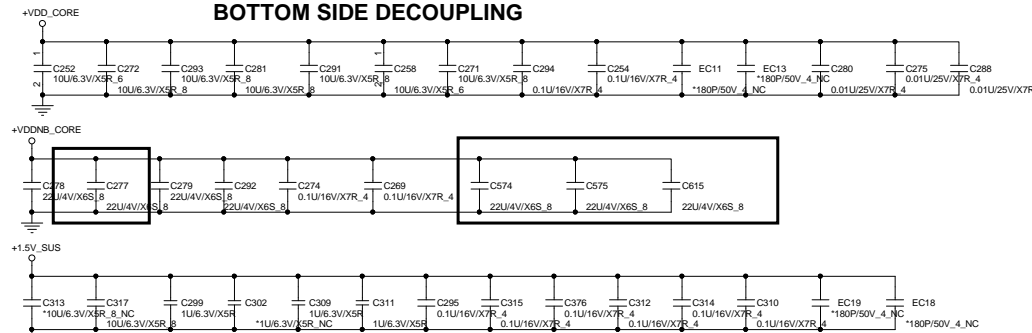
APU POWER TABLE			
PIN NAME	NET NAME	VOLTAGE	
VDD	+VDD_CORE	+1.1V	
VDDNB	+VDDNB_CORE		
VDDIO	+1.5V_SUS	+1.5V	
VDDP	+1.2V_VDDP	+1.2V	
VDDR	+1.2V_VDDR	+1.2V	
VDDA	+2.5V_VDDA	+2.5V	



Sequence  
GROUP A(VDDIO,VDDA)  
!!!  
GROUP B(VDD\_RUN, VDDNB\_RUN, VDDP, VDDR)

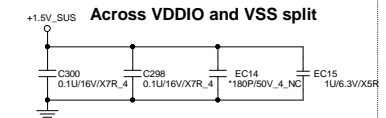


## BOTTOM SIDE DECOUPLING



If the VSS plane is cut to create a VDDIO plane, ceramic capacitors are connected across the VDDIO and VSS plane split as follows

## DECOUPLING between PROCESSOR and DIMMs

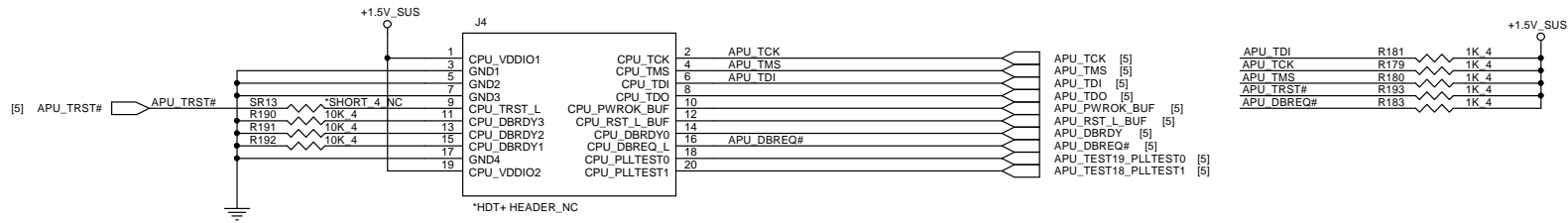


Quanta Computer Inc.

PROJECT : R0AA

Size	Document Number	Rev
	POWER/GND	B
Date:	Monday, June 25, 2012	Sheet 6 of 55

**HDT+ Connector**    Debug only  
Remove after MP



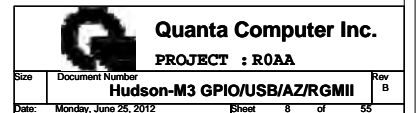
**PROJECT : R0AA**

Size	Document Number	Rev
	<b>DEBUG&amp;OTHER</b>	<b>B</b>

Date: Monday, June 25, 2012 Sheet 7 of 55

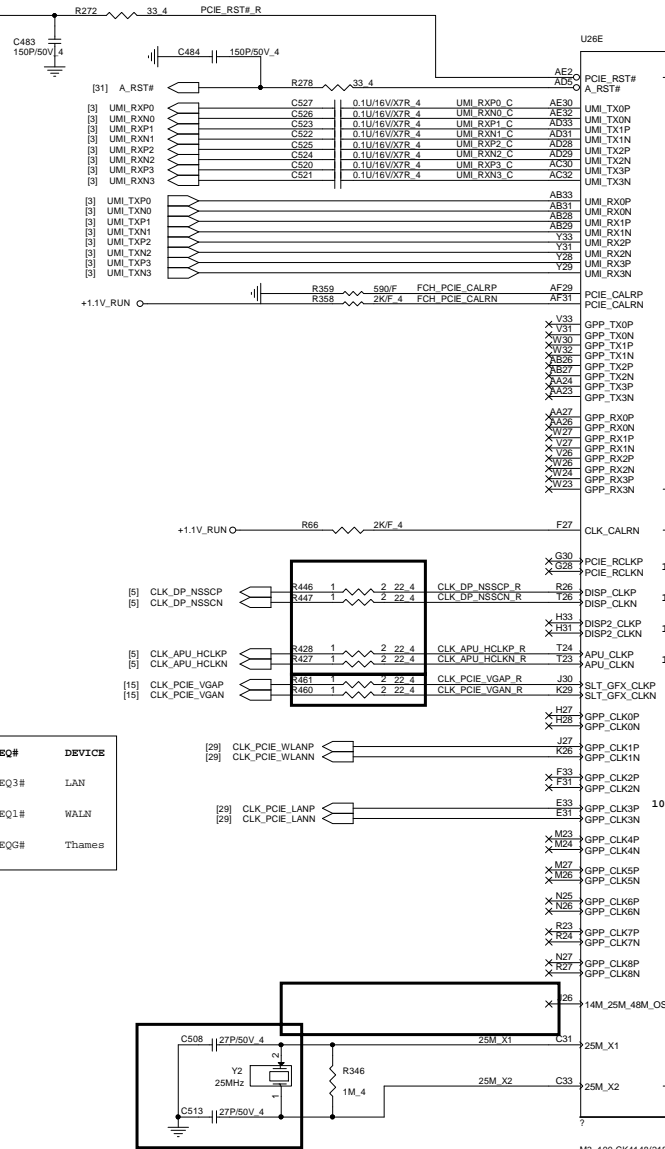
Date: Monday, June 25, 2012 Sheet 7 of 55

Date: Monday, June 25, 2012 Sheet 7 of 55





[15,27,29] APU\_PCIE\_RST#  
APU\_PCIE\_RST# is for APU PCIe devices reset



## HUDSON-M2

Part 1 of 5

PCI CLKs

PCI CLKs

PCI CLKs

PCI CLKs

PCI CLKs

PCI CLKs

PCI CLKs

PCI CLKs

PCI CLKs

PCI CLKs

PCI CLKs

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PCI CLKs

PCI CLKs

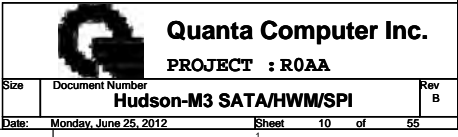
PCI CLKs

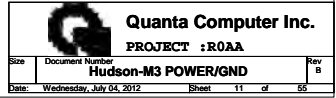
PCI CLKs

PCI CLKs

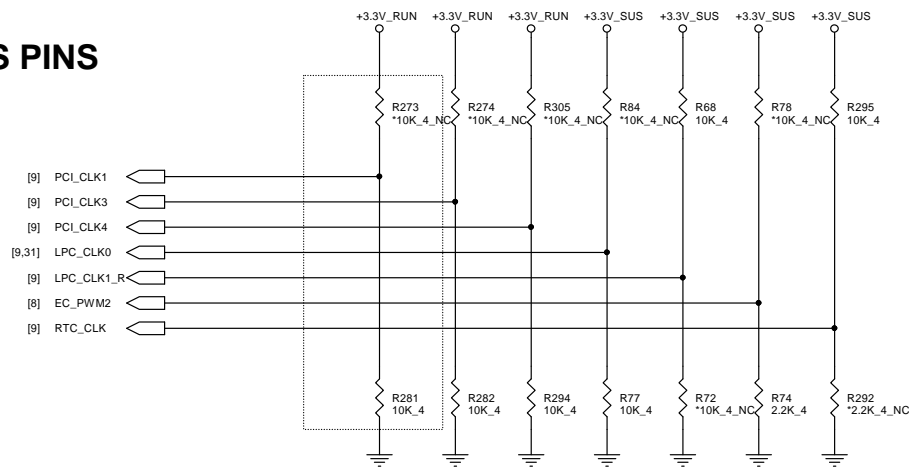
PCI CLKs

PCI CLKs





## STRAPS PINS

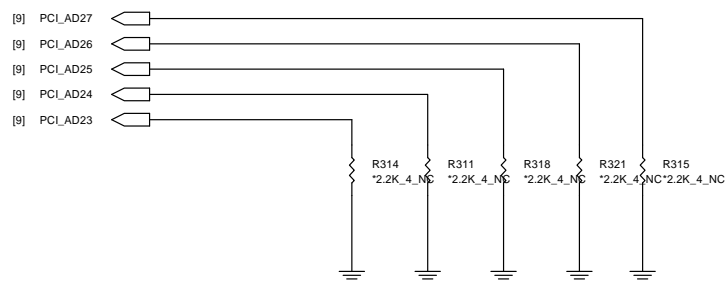


## REQUIRED STRAPS

	-----	PCI_CLK1	-----	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
<b>PULL HIGH</b>	-----	ALLOW PCIE Gen2	-----	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED  Setting	LPC ROM	S5 PLUS MODE DISABLED  Setting
<b>PULL LOW</b>	-----	FORCE PCIE Gen1 Setting	-----	IGNORE DEBUG STRAP Setting	FUSION CLOCK MODE Setting	EC DISABLED Setting	CLKGEN DISABLED	SPI ROM Setting	S5 PLUS MODE ENABLED

## DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI\_AD[27:23]



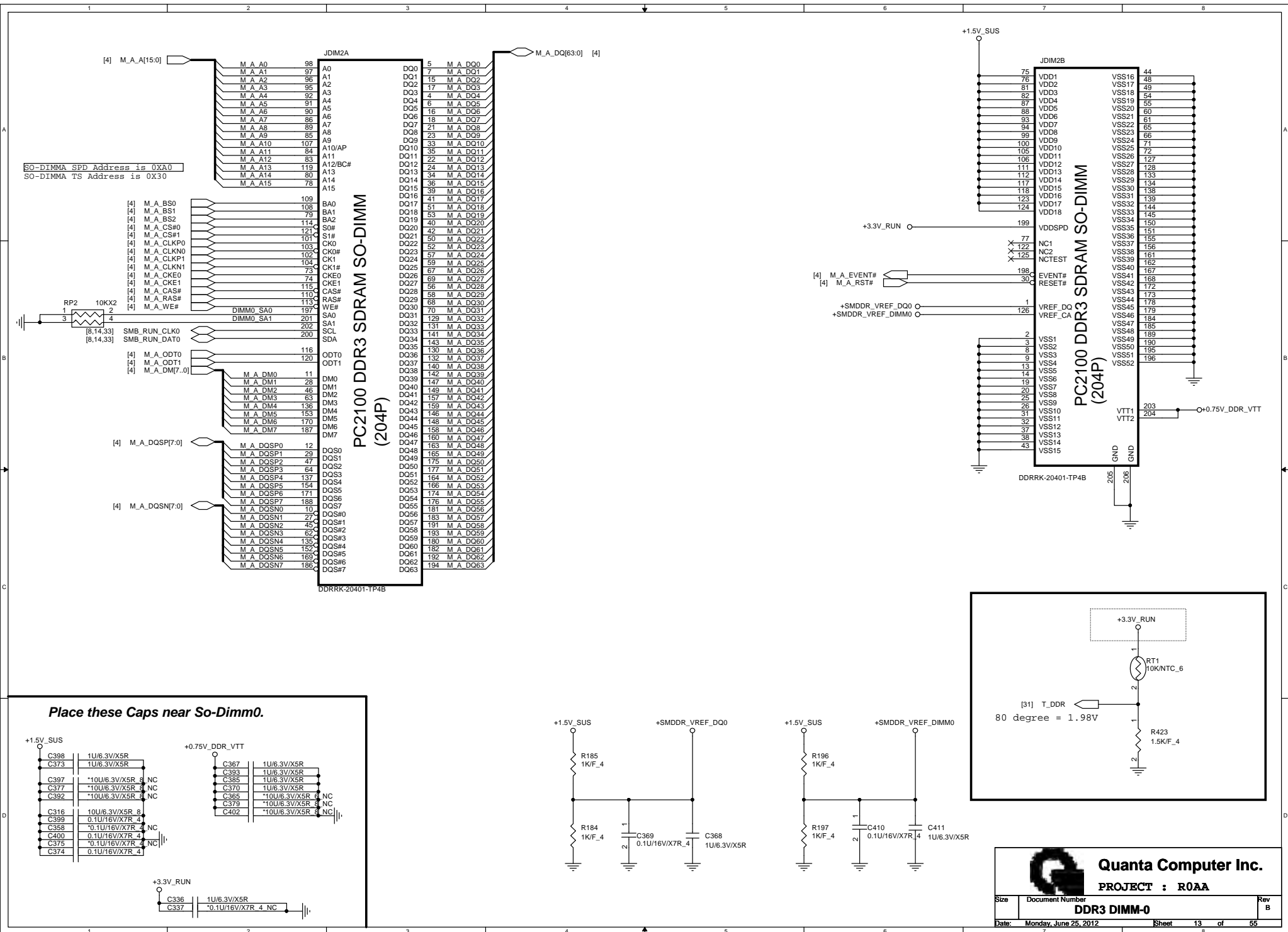
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
<b>PULL HIGH</b>	USE PCI PLL Setting	DISABLE ILA AUTORUN Setting	USE FC PLL Setting	USE DEFAULT PCIE STRAPS Setting	DISABLE PCI MEM BOOT Setting
<b>PULL LOW</b>	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

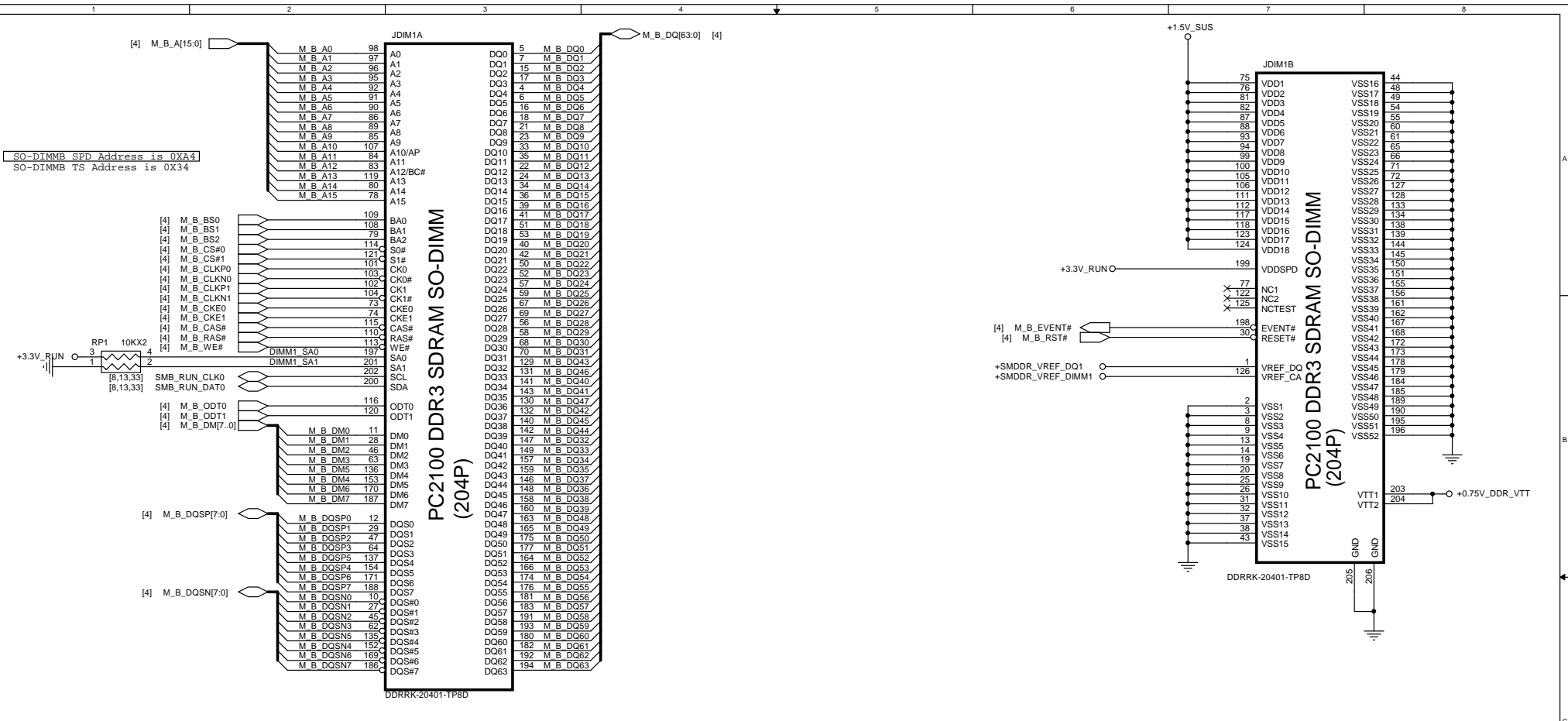


**Quanta Computer Inc.**

**PROJECT : R0AA**

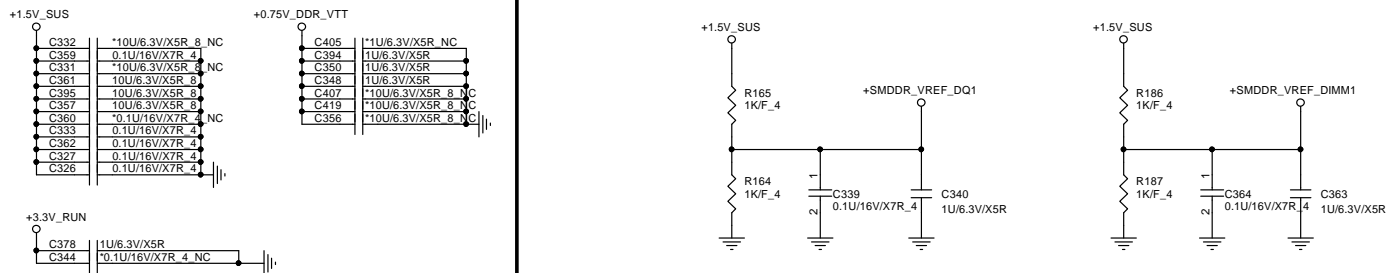
Size	Document Number	Rev
	<b>Hudson-M3 STRAP/PWRGD</b>	<b>B</b>
Date:	Monday, June 25, 2012	Sheet 12 of 55





Place these Caps near So-Dimm1.

CH6101M9905  
CAP CHIP 100 6.3V(+/-20%,X5R,0603)



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**PROJECT : R0AA**

Size	Document Number	Rev
	<b>DDR3 DIMM-1</b>	B

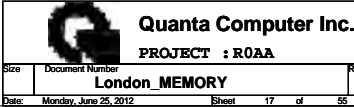
Date: Monday, June 25, 2012 Sheet 14 of 55

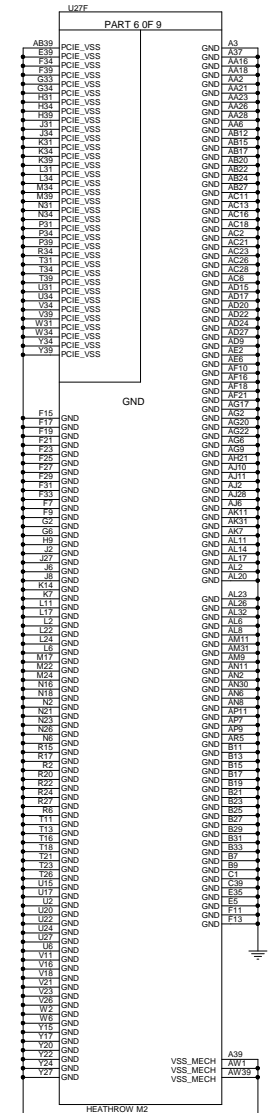




**WWW.AliSaler.Com**





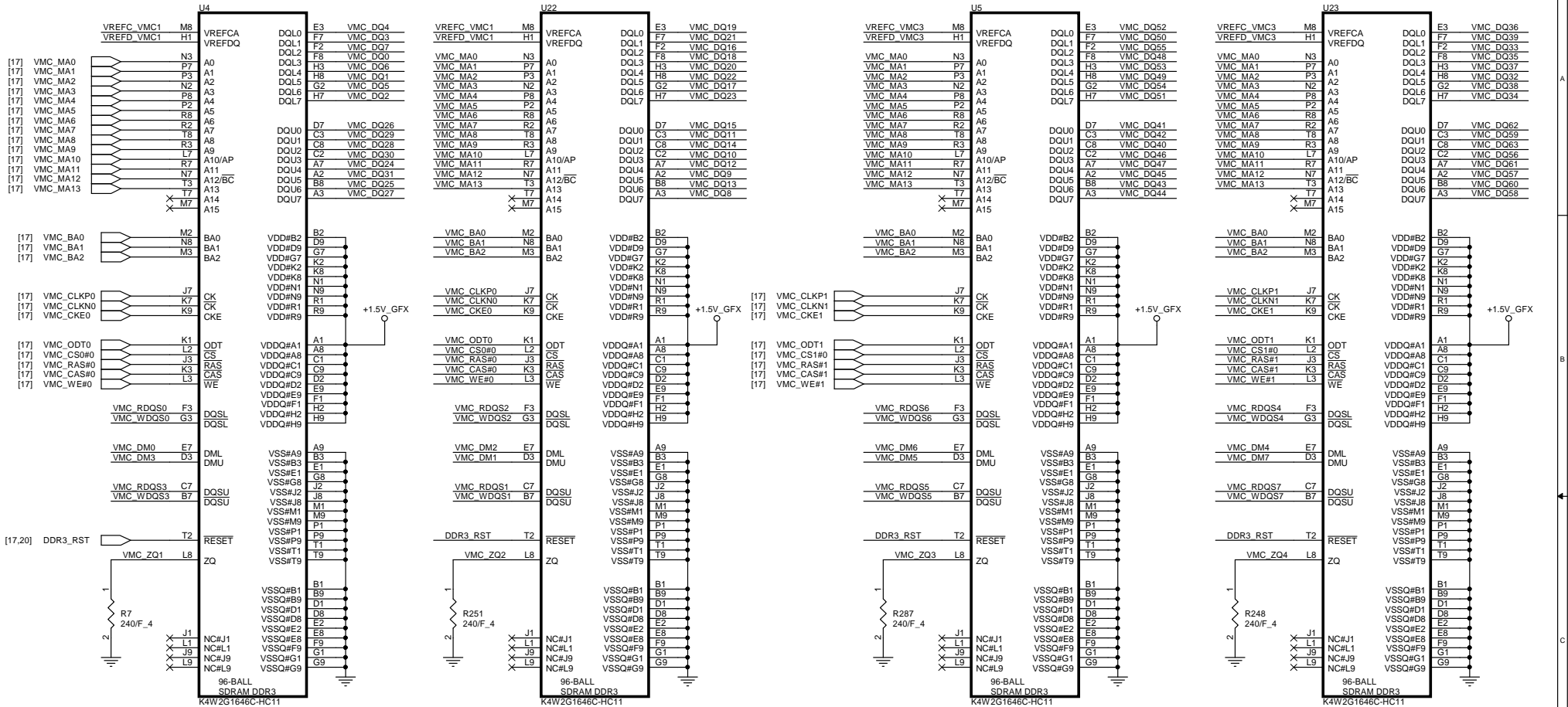




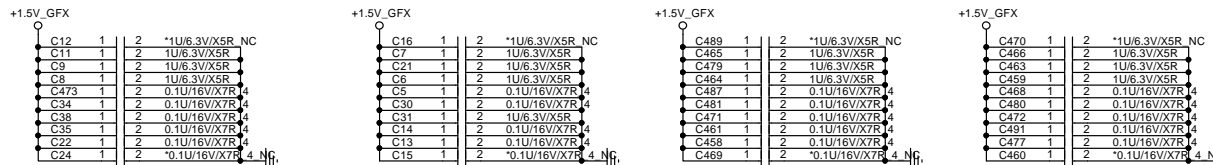
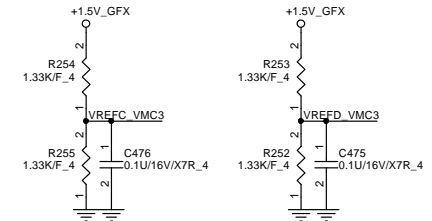
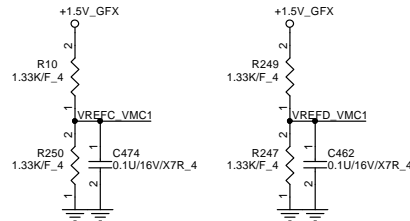
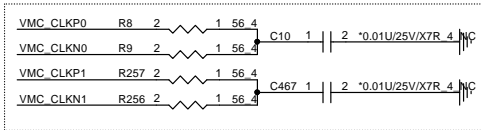


# CHANNEL B: 1024MB DDR3

[17] VMC\_MA[13..0]  
[17] VMC\_DQ[63..0]  
[17] VMC\_DM[7..0]  
[17] VMC\_WDQS[7..0]  
[17] VMC\_RDQS[7..0]

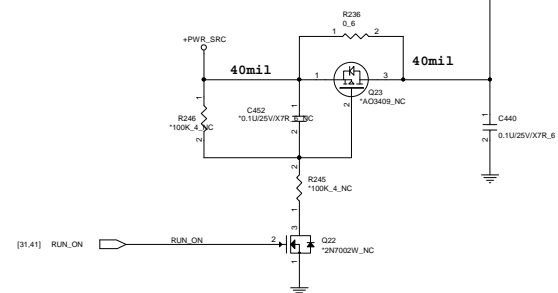
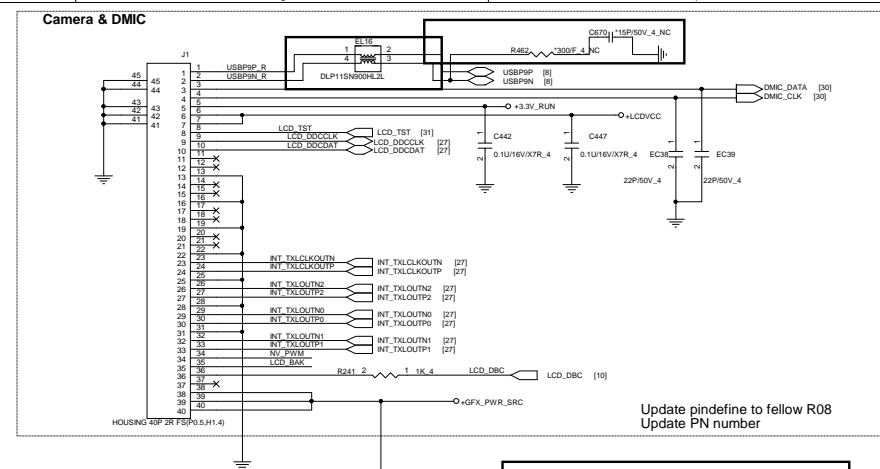
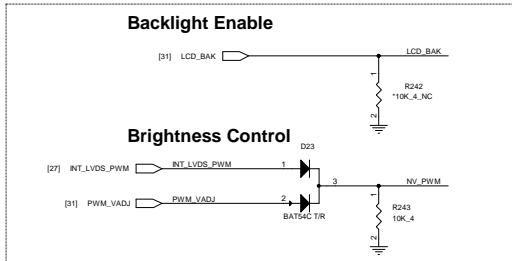
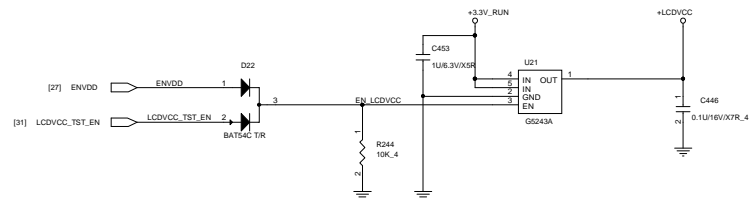


Placement has to be close to VRAM



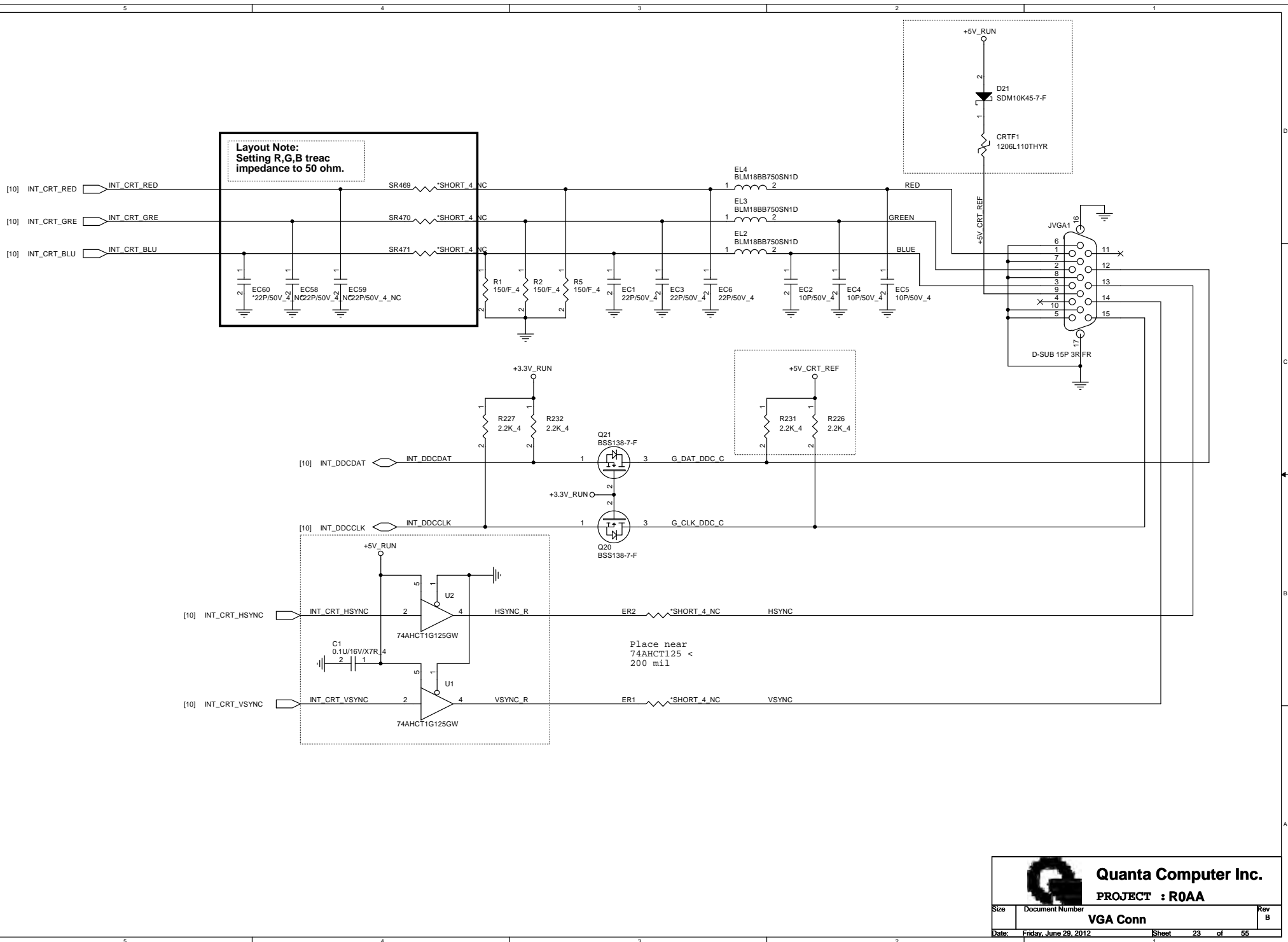
**Quanta Computer Inc.**  
PROJECT : R0AA

Size	Document Number	Rev
	N11M-GE2 VRAM-2(DDR3 BGA96)	1A
Date:	Monday, June 25, 2012	Sheet 21 of 55

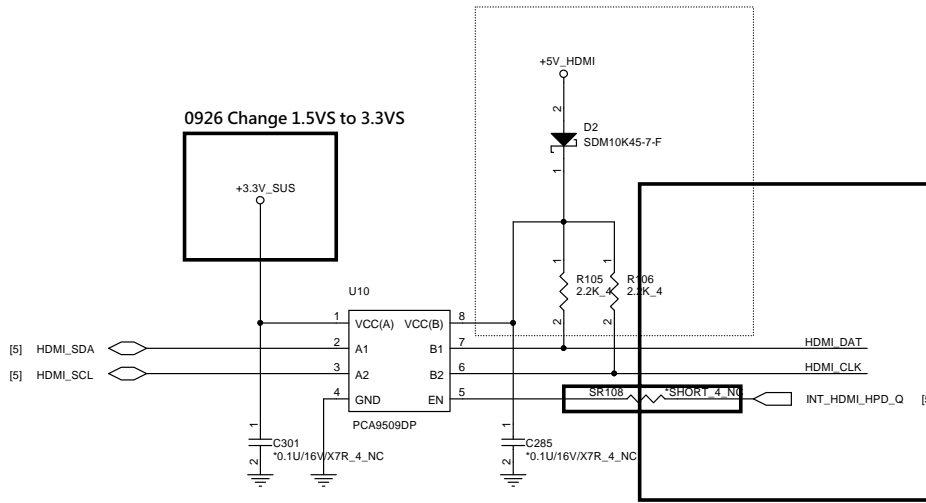


### EMC Reserve

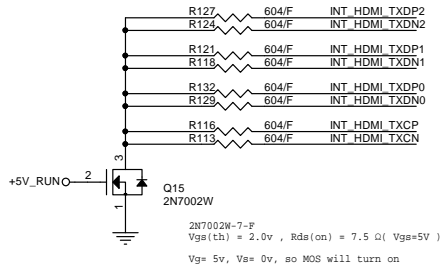
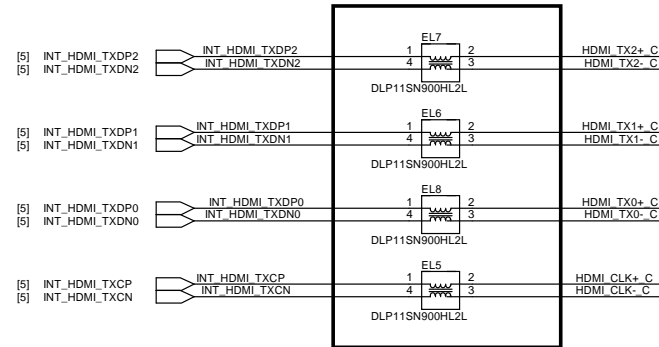
INT_TXCLKOUTN	ER18	1	2	3.3P	INT_TXCLKOUTP
INT_TXLQUTN2	ER16	1	2	3.3P	INT_TXLQUTP2
INT_TXLQUTN1	ER17	1	2	3.3P	INT_TXLQUTP1
INT_TXLQUTN0	ER19	1	2	3.3P	INT_TXLQUTP0



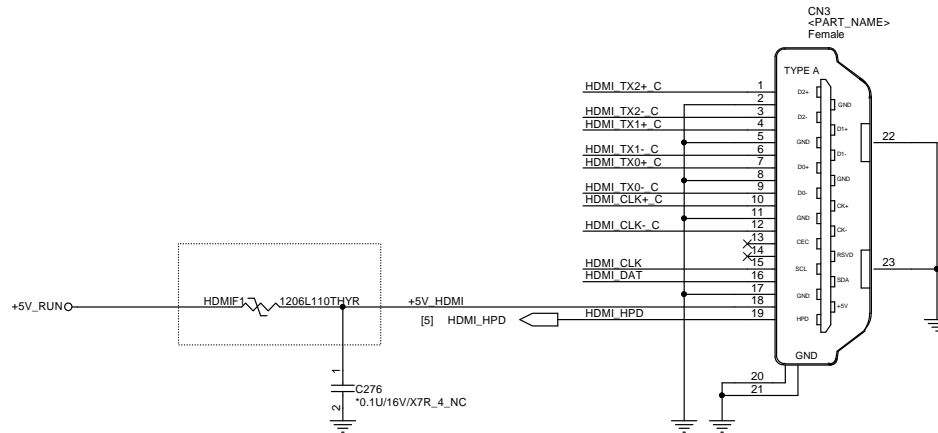
0926 Change 1.5VS to 3.3VS



Reserve for EMI and close to HDMI CONN



HDMI Conn.



Quanta Computer Inc.  
PROJECT : R0AA

Size Document Number Rev B  
HDMI CONN  
Date: Thursday, June 28, 2012 Sheet 24 of 55



S	OE	Function
X	H	Disconnect
L	L	D=1D
H	L	D=2D

## USB Power share

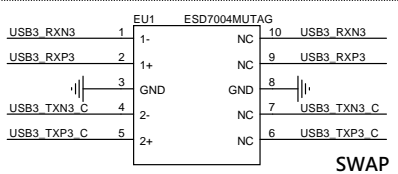
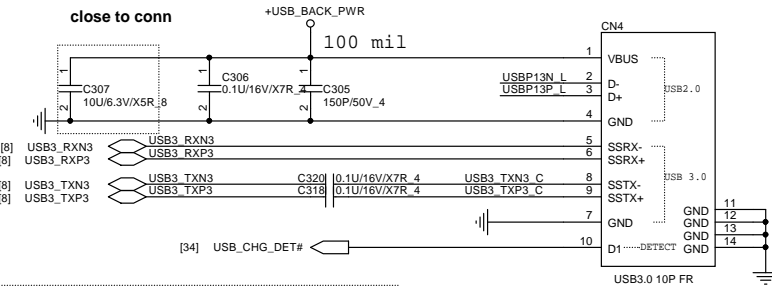
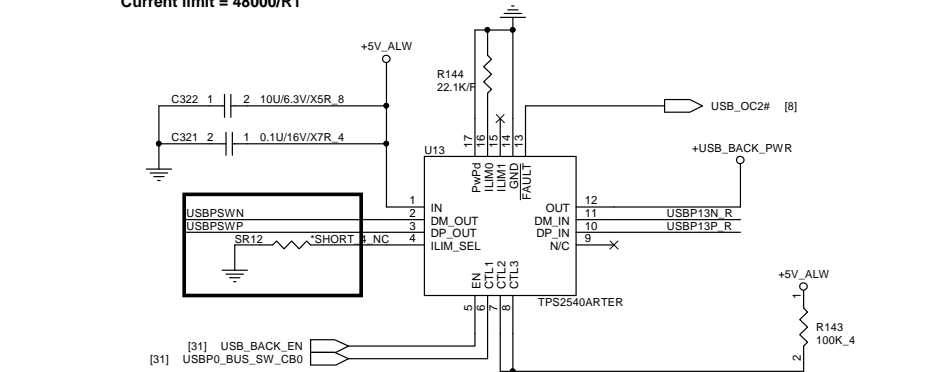
USBP0_BUS_SW_CB0	Mode
Low	DCP, Auto-detect
High	CDP, BC Spec 1.1

	R1	mA
OC limitation	100k ohm	480
	22.1k ohm	2171

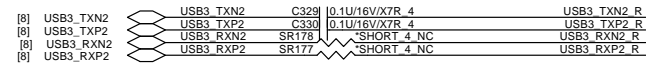
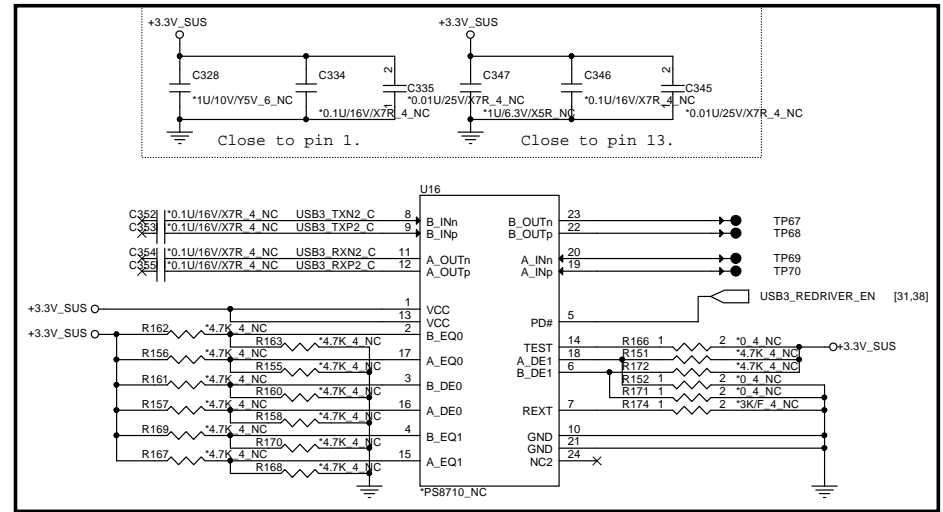
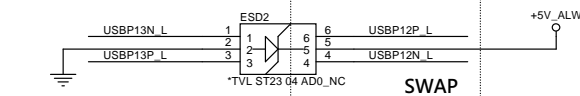
**Applied Now**

Current limit = 48000/R1

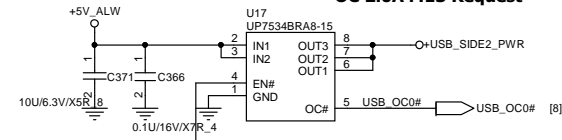


## ESD Function

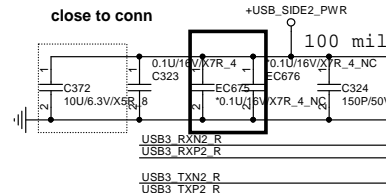
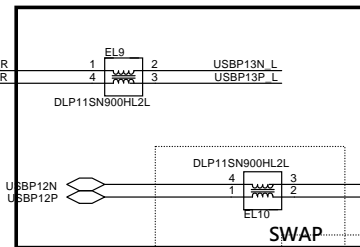
Place ESD diodes as close as USB connector.



## I continuous 1.5A OC 2.0A M13 Request



[29,31,38] USB\_RIGHT\_EN#



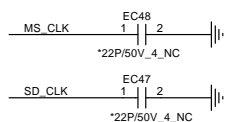
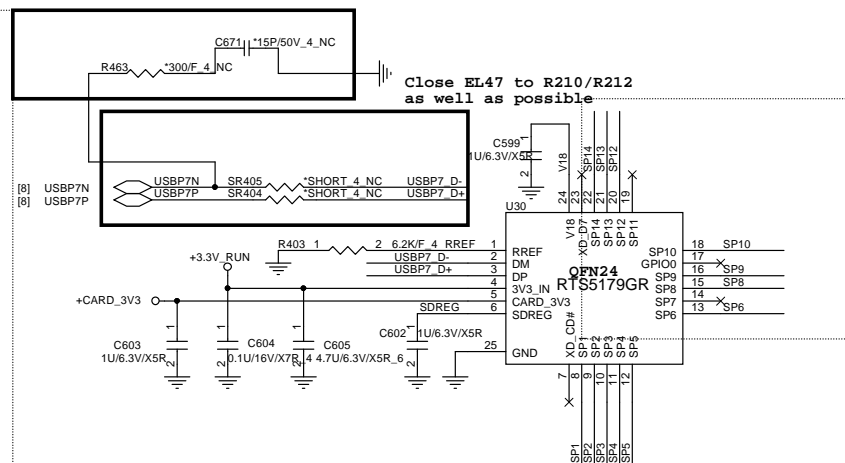
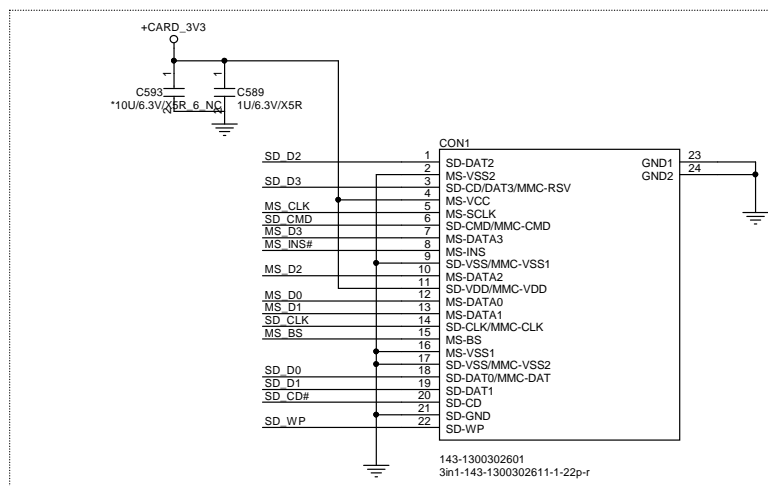
**Quanta Computer Inc.**  
PROJECT : R0AA

Size Document Number  
**USB 3.0 port / USB power share**

Date: Thursday, June 28, 2012 Sheet 25 of 55

# Cardreader (RTS5179GR) Support SD3.0 USH50

Change CON1 footprint to 3in1-143-1300302611-1-22p-r(follow R09)



SP1	SD_WP	MS_CLK
SP2	SD_D1	MS_INS#
SP3	SD_D0	MS_D7
SP4	SD_D7	MS_D3
SP5	SD_CD#	
SP6		
SP8	SD_CLK	MS_D2
SP9	SD_D5	MS_D0
SP10	SD_CMD	
SP12	SD_D3	MS_D1
SP13	SD_D2	MS_D5
SP14		MS_BS

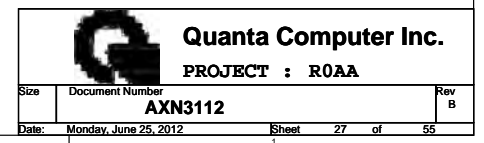
## Share Pin

	SD CARD	MS CARD
SP1	SW_WP	MS_CLK
SP2		MS_INS#
SP3	SD_D1	
SP4	SD_D0	MS_D7
SP5	SD_D7	MS_D3
SP6	SD_CD#	
SP7	SD_D6	MS_D6
SP8	SD_CLK	MS_D2
SP9	SD_D5	MS_D0
SP10	SD_CMD	
SP11	SD_D4	MS_D4
SP12	SD_D3	MS_D1
SP13	SD_D2	MS_D5
SP14		MS_BS

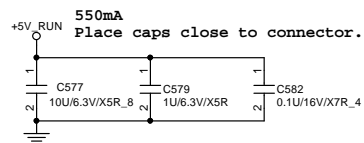
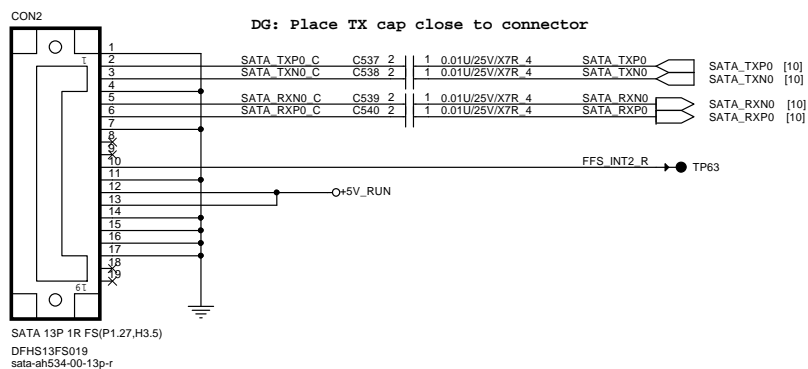


Quanta Computer Inc.  
PROJECT : R0AA

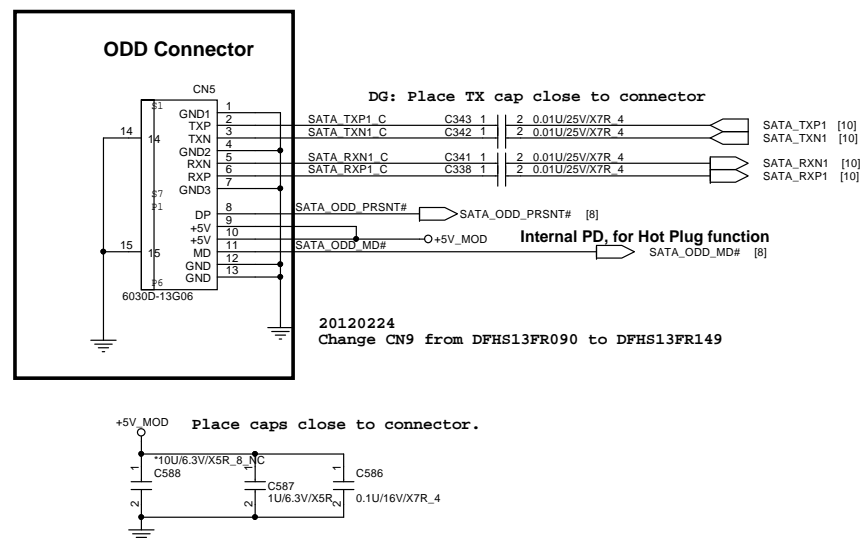
Size	Document Number	Rev
	Cardreader (RTS5179GR)	1A
Date:	Thursday, June 28, 2012	Sheet 26 of 55



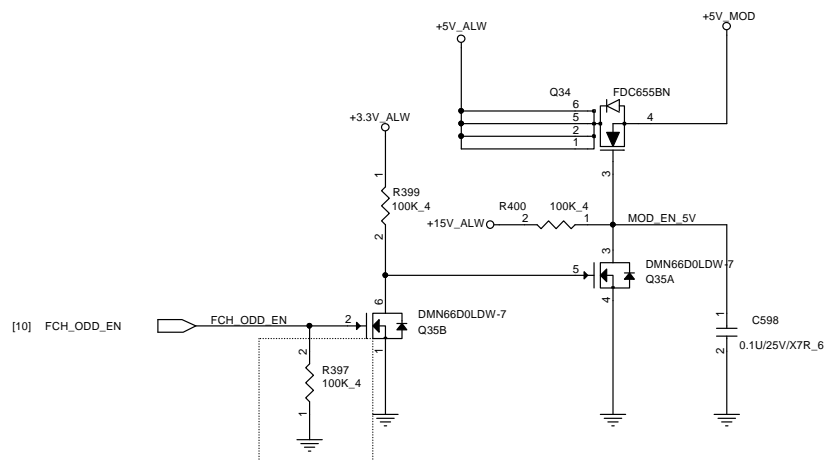
## HDD



## ODD

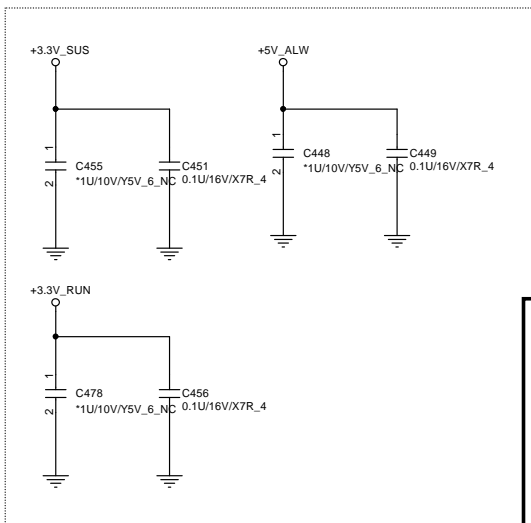


## Support Zero power ODD



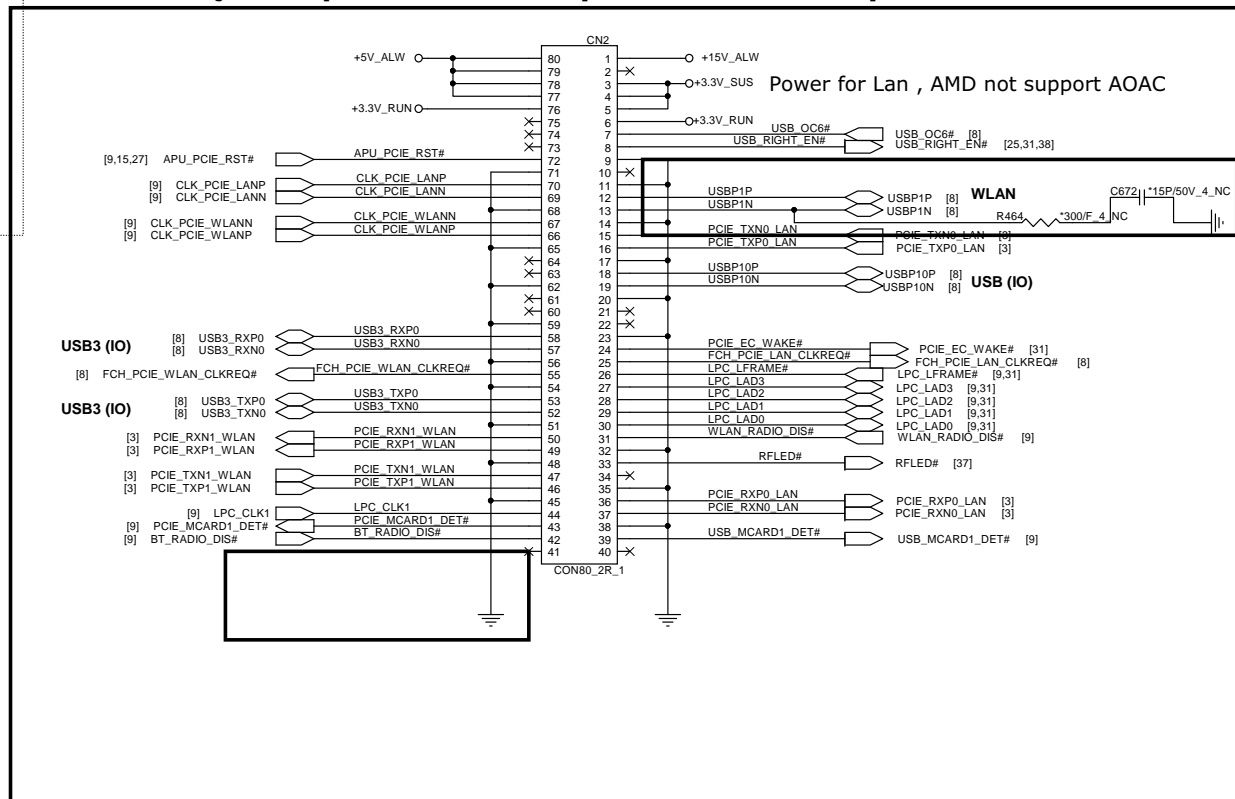
**Quanta Computer Inc.**  
**PROJECT : R0AA**

Size	Document Number	Rev
	<b>SATA HDD/ODD</b>	B
Date:	Monday, June 25, 2012	Sheet 28 of 55



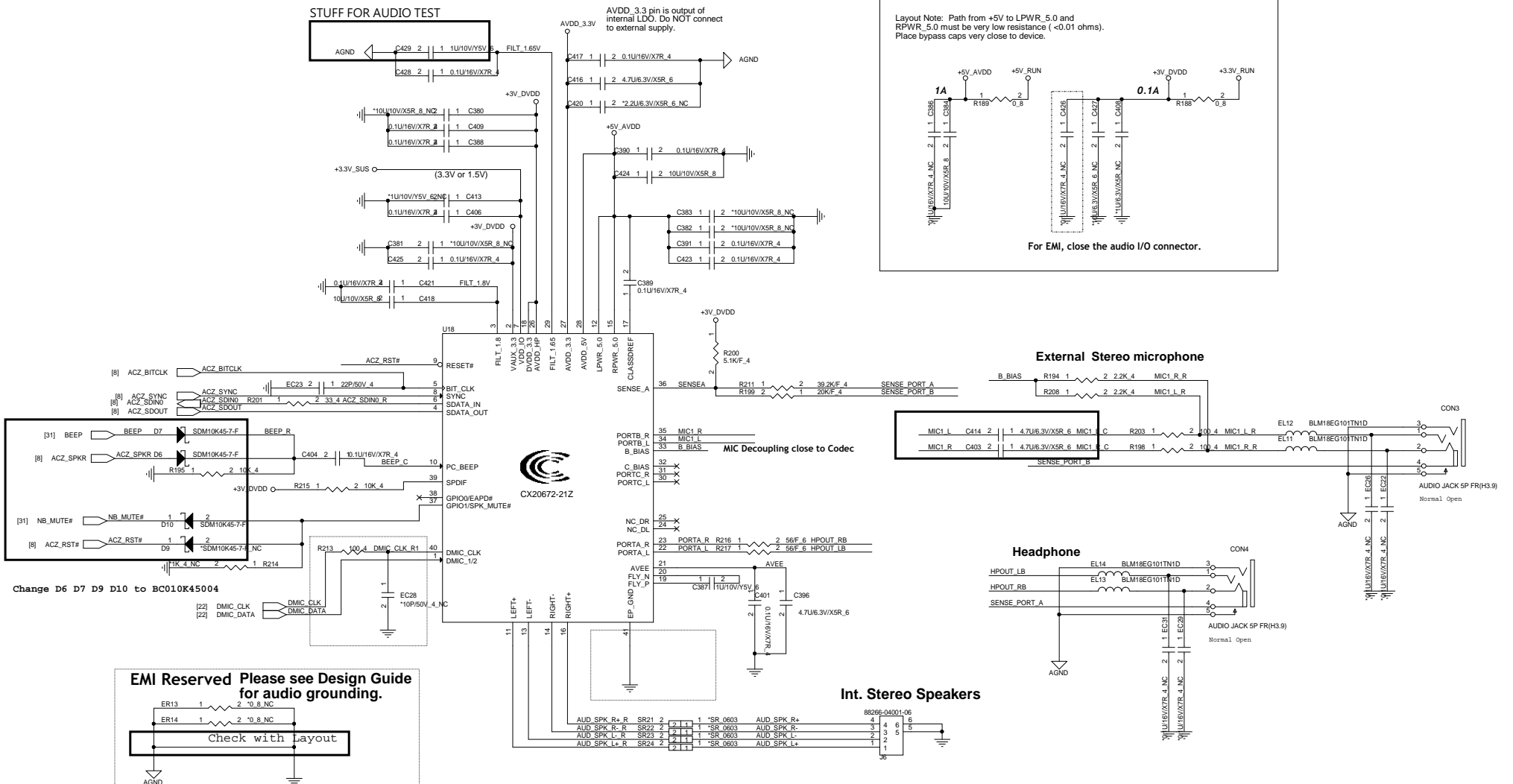
20120229

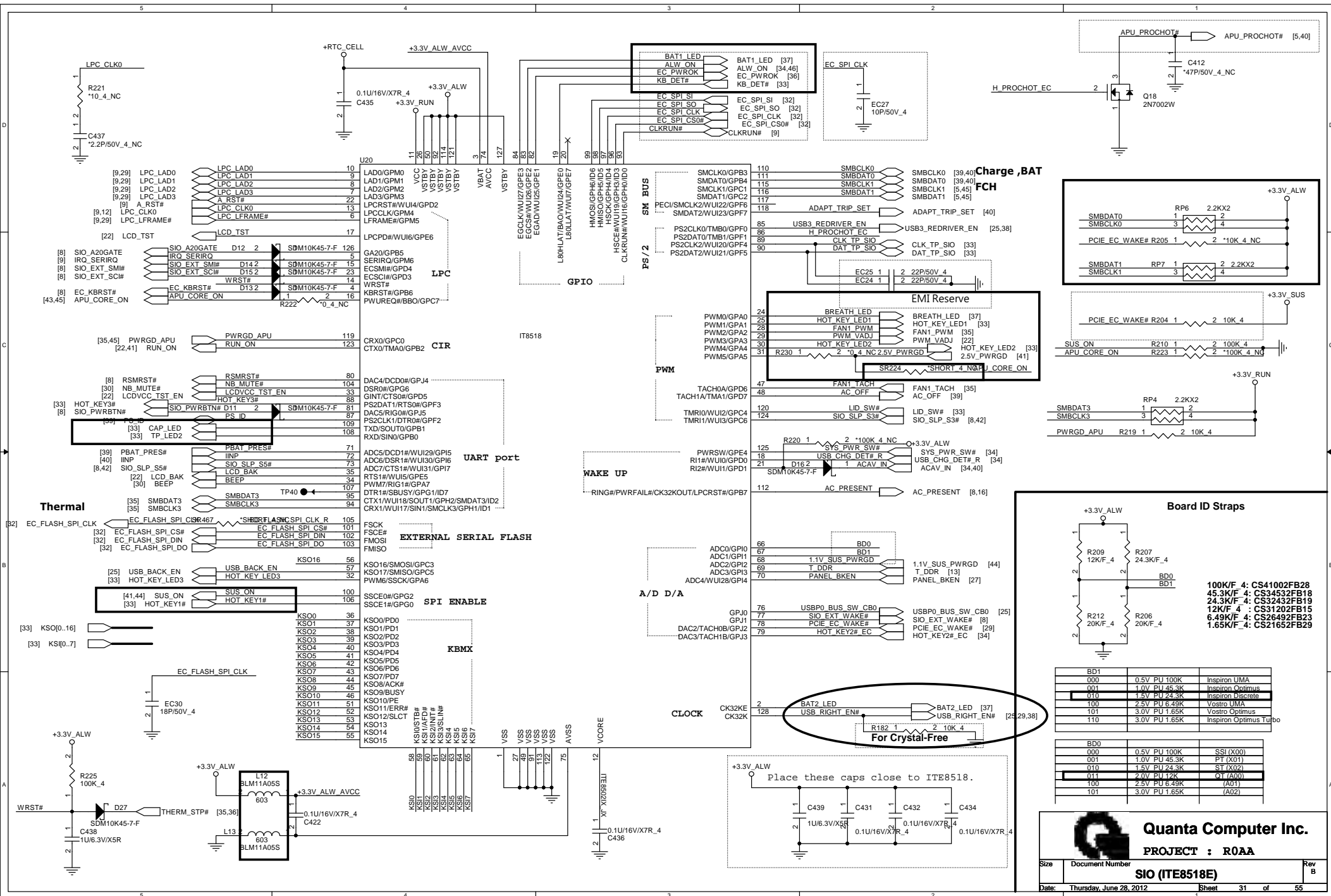
Change CN9 footprint from "88161-08001-80p-ldh" to "88069-8001b-bs-80p-ldh-smt"



Quanta Computer Inc.  
PROJECT : R0AA

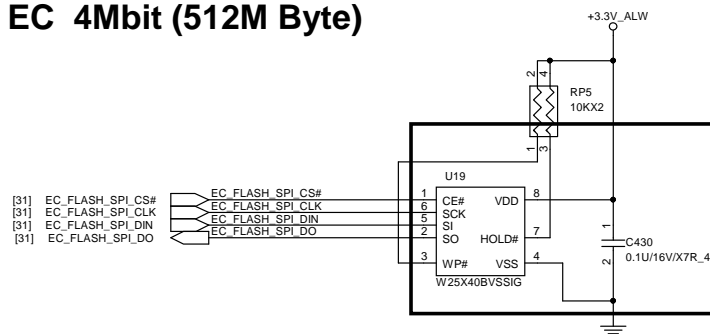
Size	Document Number	Rev
	BTB CONN	B
Date: Monday, June 25, 2012	Sheet 29 of 55	



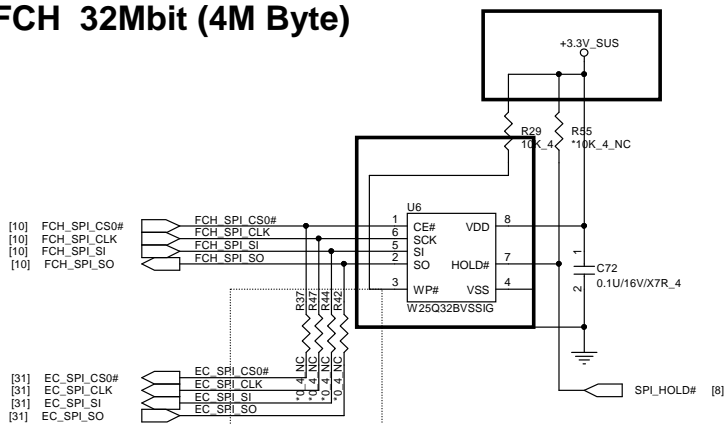


# FLASH / RTC

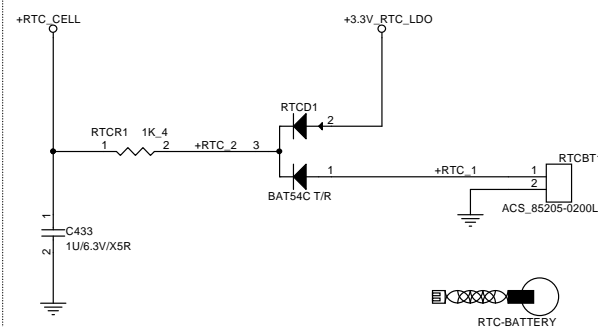
## For EC 4Mbit (512M Byte)



## For FCH 32Mbit (4M Byte)



## RTC



Double, 25°C, Vf=0.4V, If=25mA  
one, 25°C, Vf=0.35V, If=15.8mA



Quanta Computer Inc.

PROJECT : R0AA

Size Document Number

FLASH / RTC

Rev

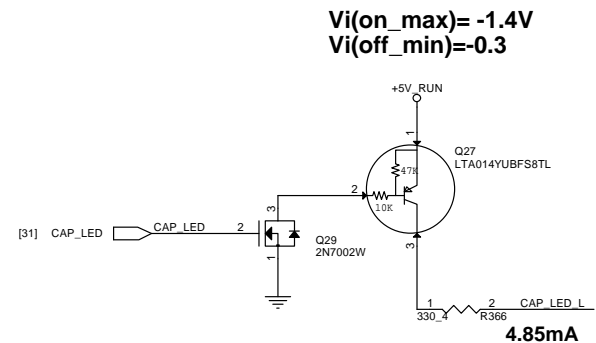
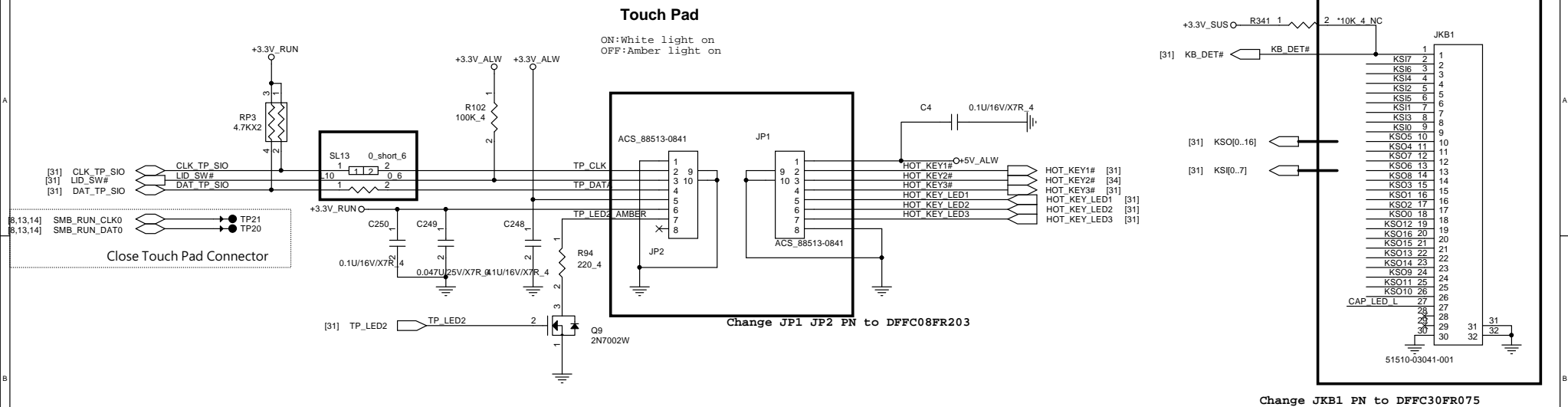
B

Date: Monday, June 25, 2012

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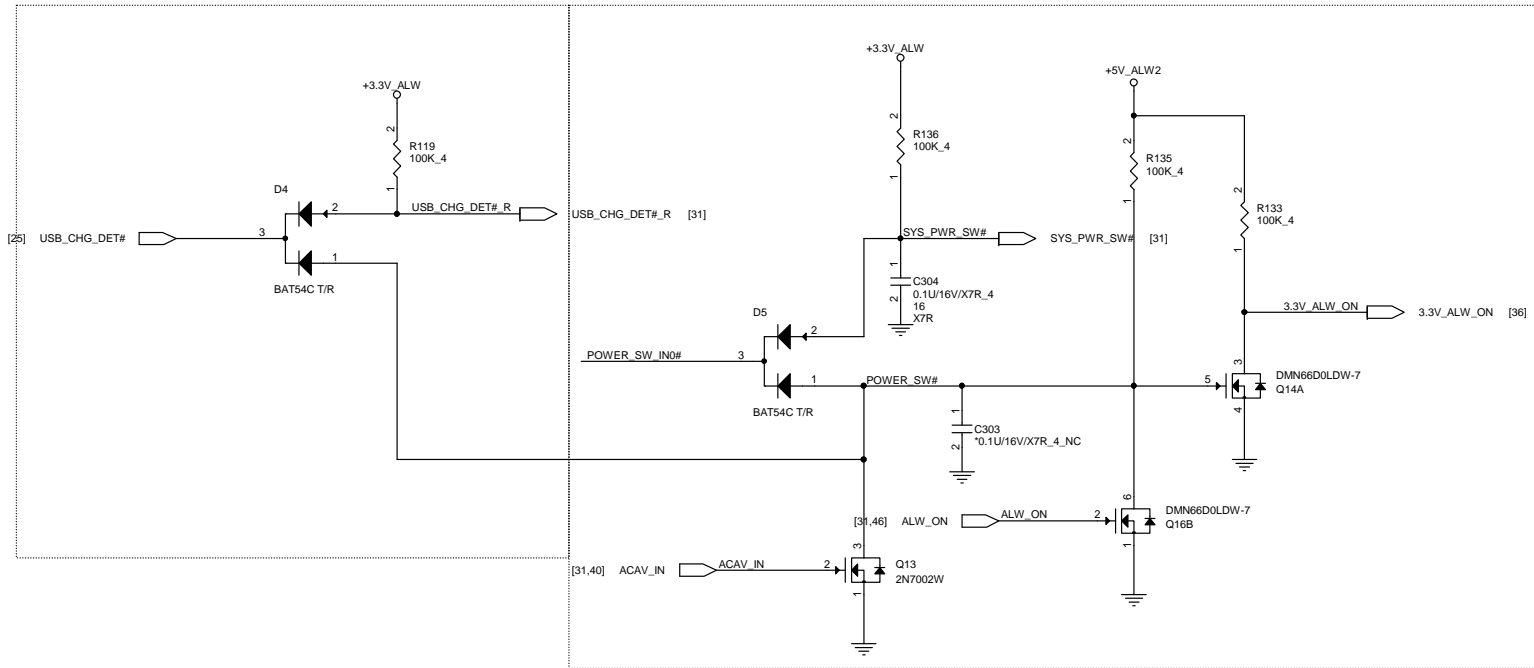


# KEYBOARD CONNECTOR

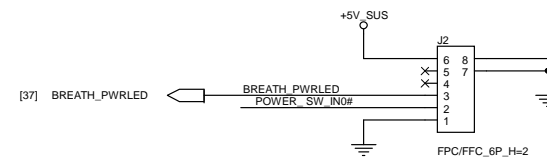
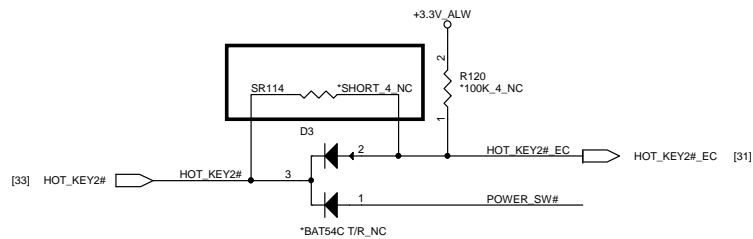


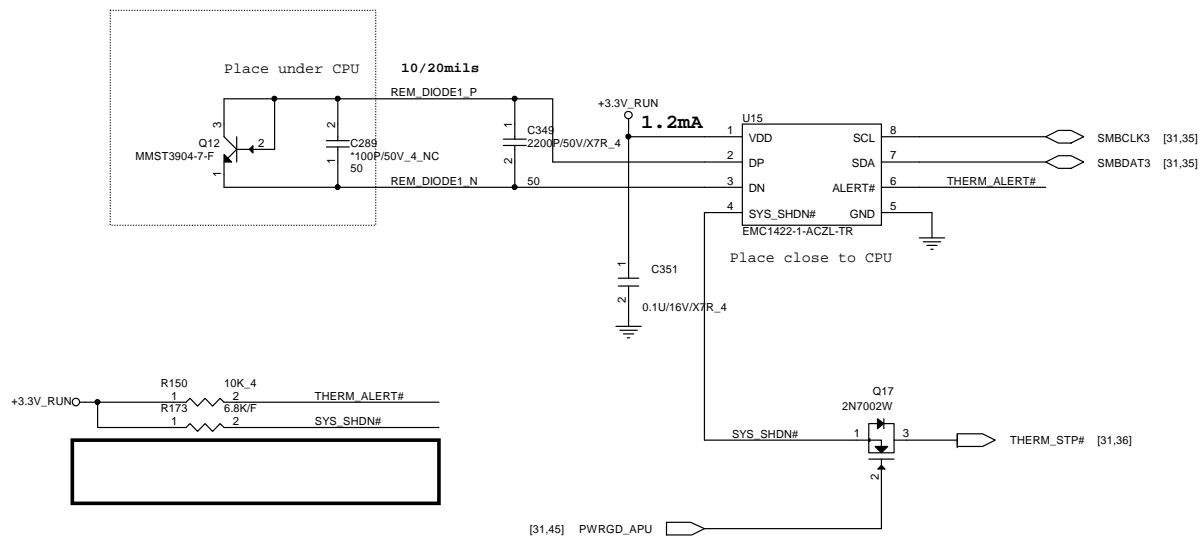
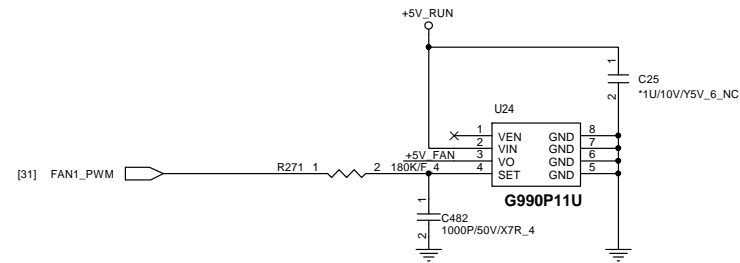
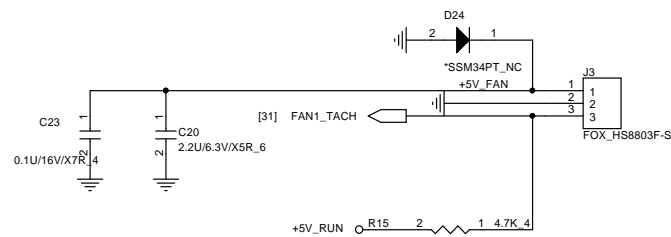
## For USB charger usage

## 3V ALW ON POWER LOGIC

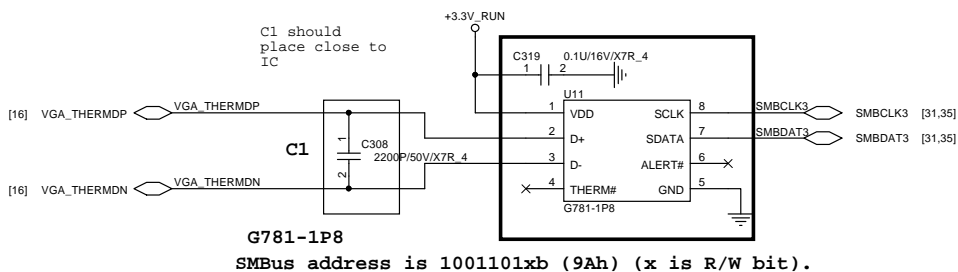


## TO PWR button board

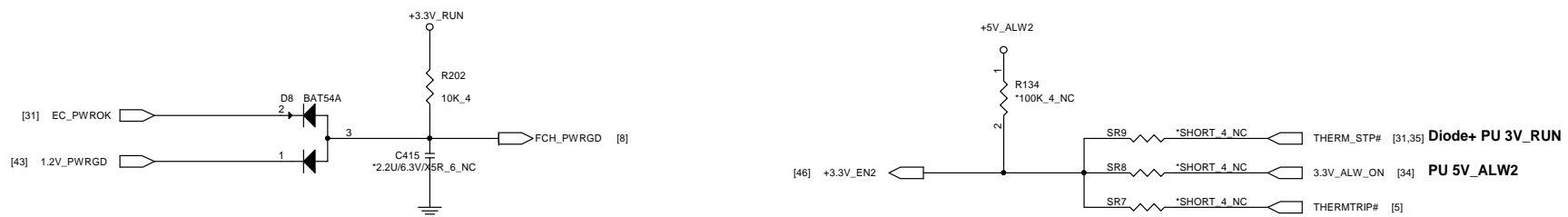


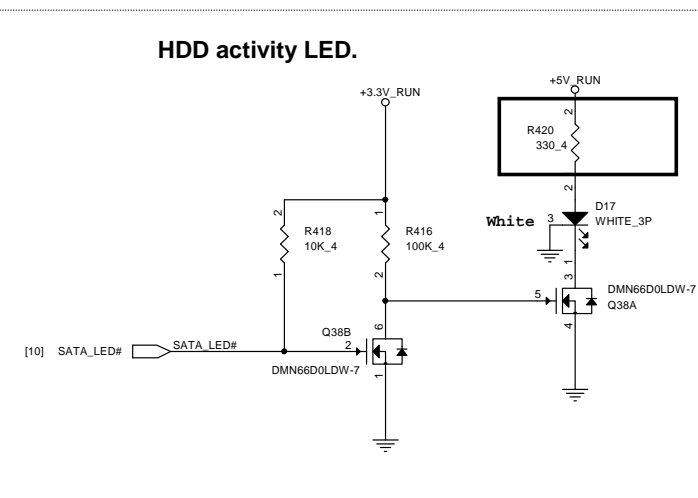
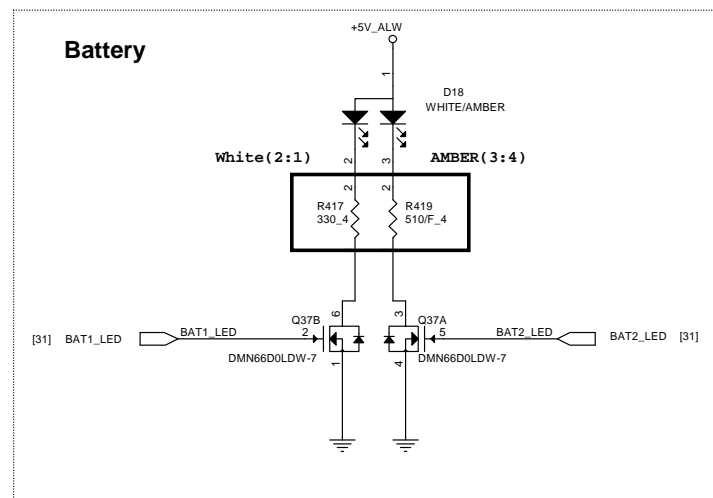
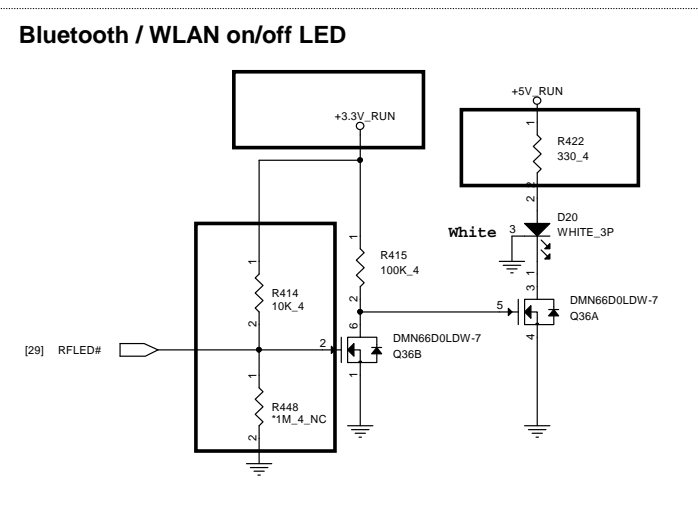
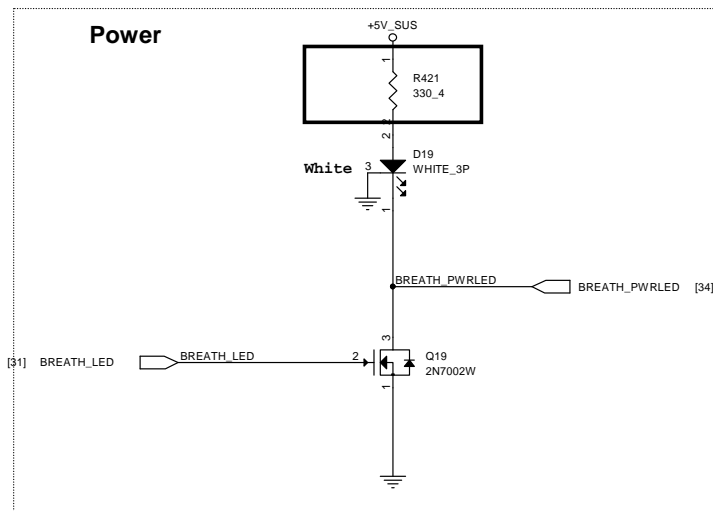


SYS_SHDN#	4.7K	6.8K	10K	15K	22K	33K
ALERT#						
4.7K	77 °C	83 °C	89 °C	95 °C	101 °C	107 °C
6.8K	78 °C	84 °C	90 °C	96 °C	102 °C	108 °C
10K	79 °C	85 °C	91 °C	97 °C	103 °C	109 °C
15K	80 °C	86 °C	92 °C	98 °C	104 °C	110 °C
22K	81 °C	87 °C	93 °C	99 °C	105 °C	111 °C
33K	82 °C	88 °C	94 °C	100 °C	106 °C	112 °C

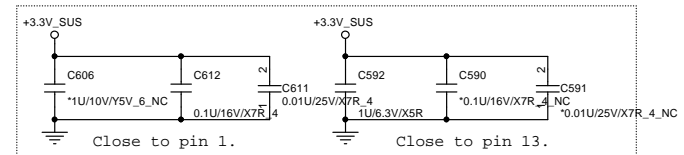
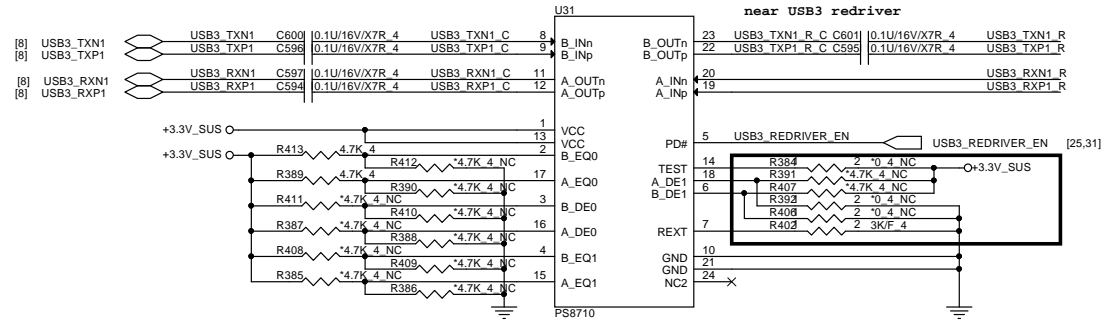
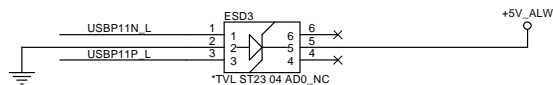
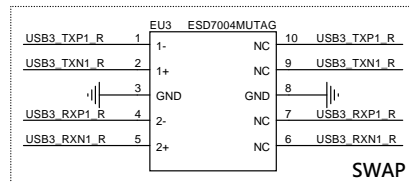
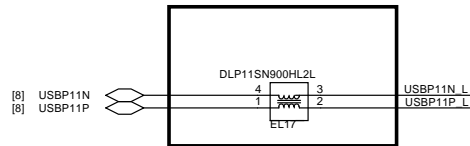
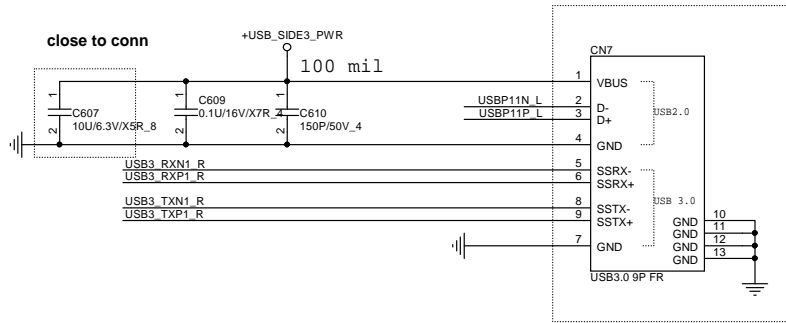
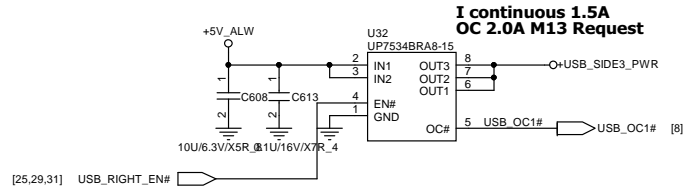


G781-1P8  
SMBus address is 1001101xb (9Ah) (x is R/W bit).





Del Colay reserve



Chip test mode enable.  
3.3V tolerant. Internally pulled down at ~ 150K ohm  
TEST =  
L: Normal operation (default)  
H: Test mode enable

Programmable output pre-emphasis level setting for channel A  
3.3V tolerant. Internally pulled down at ~ 150K ohm  
[A, DE1, A, DE0] =  
LL: 3.5dB de-emphasis  
LH: No de-emphasis  
HL: 7dB de-emphasis with boost output swing  
HH: 5dB de-emphasis with boost output swing

Programmable output pre-emphasis level setting for channel B  
3.3V tolerant. Internally pulled down at ~ 150K ohm  
[B, DE1, B, DE0] =  
LL: 3.5dB de-emphasis  
LH: No de-emphasis  
HL: 7dB de-emphasis with boost output swing  
HH: 5dB de-emphasis with boost output swing

Equalizer control and program for channel A  
3.3V tolerant. Internally pulled down at ~ 150K ohm  
[A, EQ1, A, EQ0] =  
LL: adaptive EQ enable  
LH: program EQ for channel loss up to 7dB  
HL: program EQ for channel loss up to 14.5dB  
HH: program EQ for channel loss up to 11.5dB

Equalizer control and program for channel B  
3.3V tolerant. Internally pulled down at ~ 150K ohm  
[B, EQ1, B, EQ0] =  
LL: adaptive EQ enable  
LH: program EQ for channel loss up to 7dB  
HL: program EQ for channel loss up to 14.5dB  
HH: program EQ for channel loss up to 11.5dB

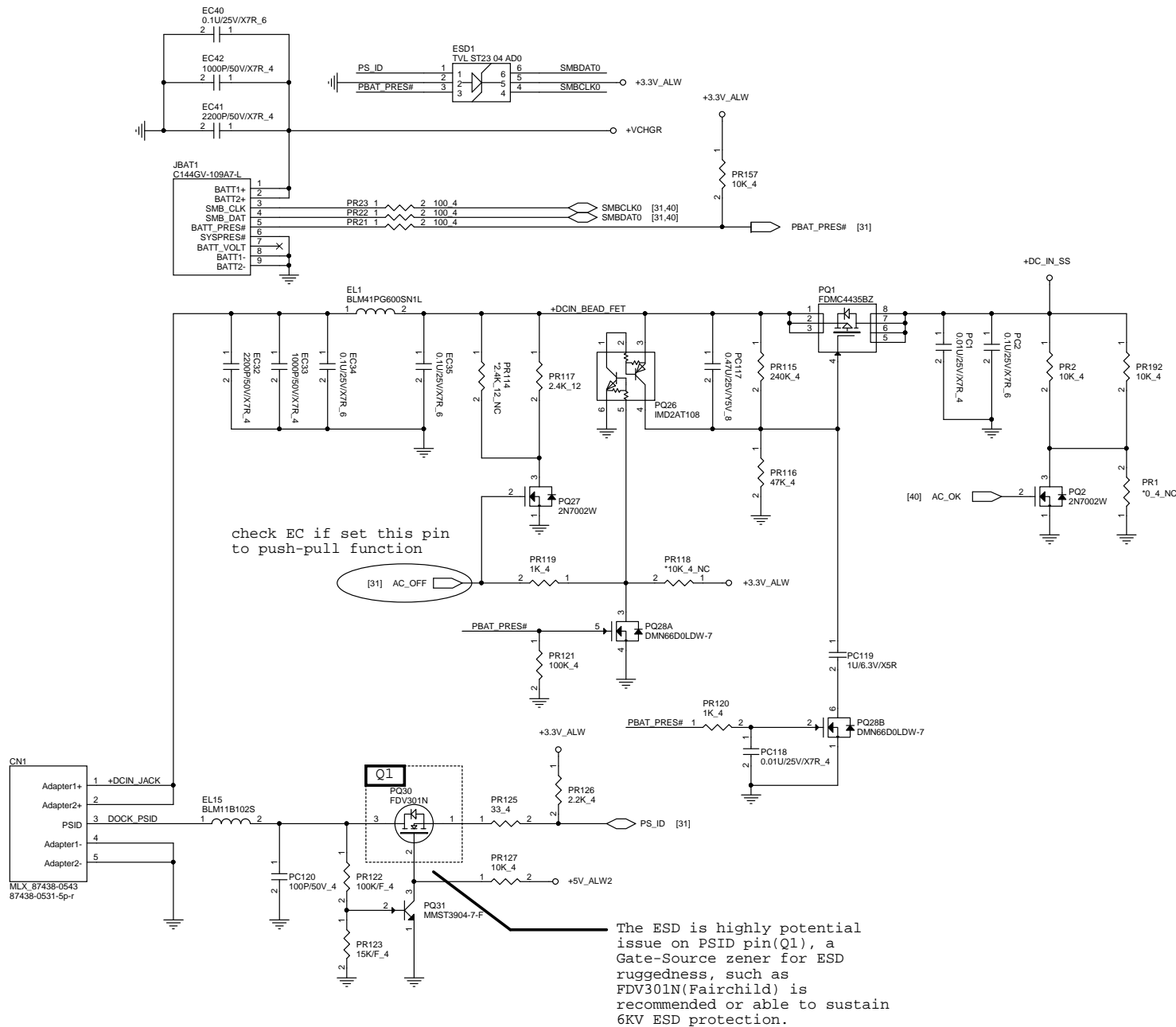


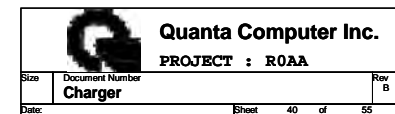
**Quanta Computer Inc.**

**PROJECT : R0AA**

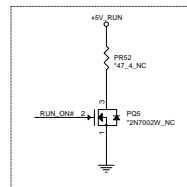
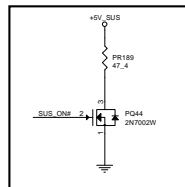
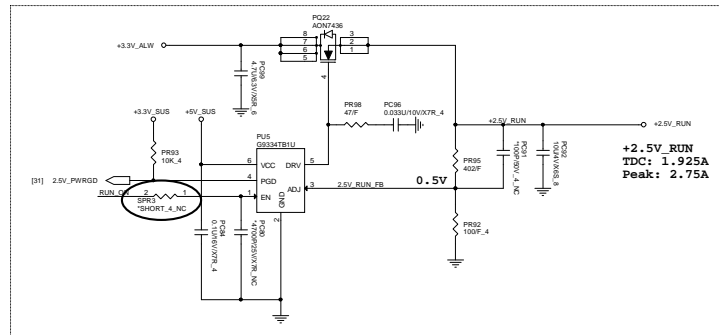
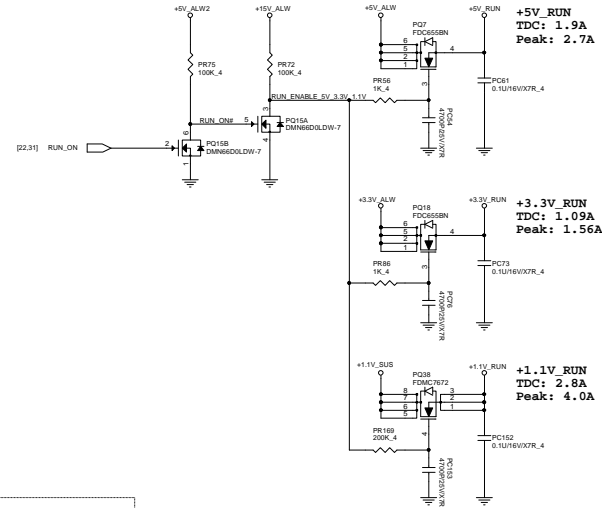
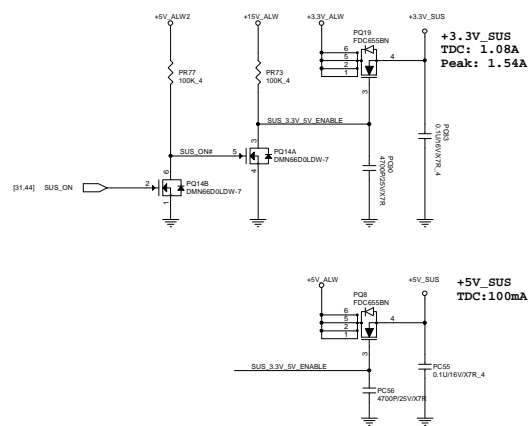
Size Document Number **USB 3.0 Left** Rev B

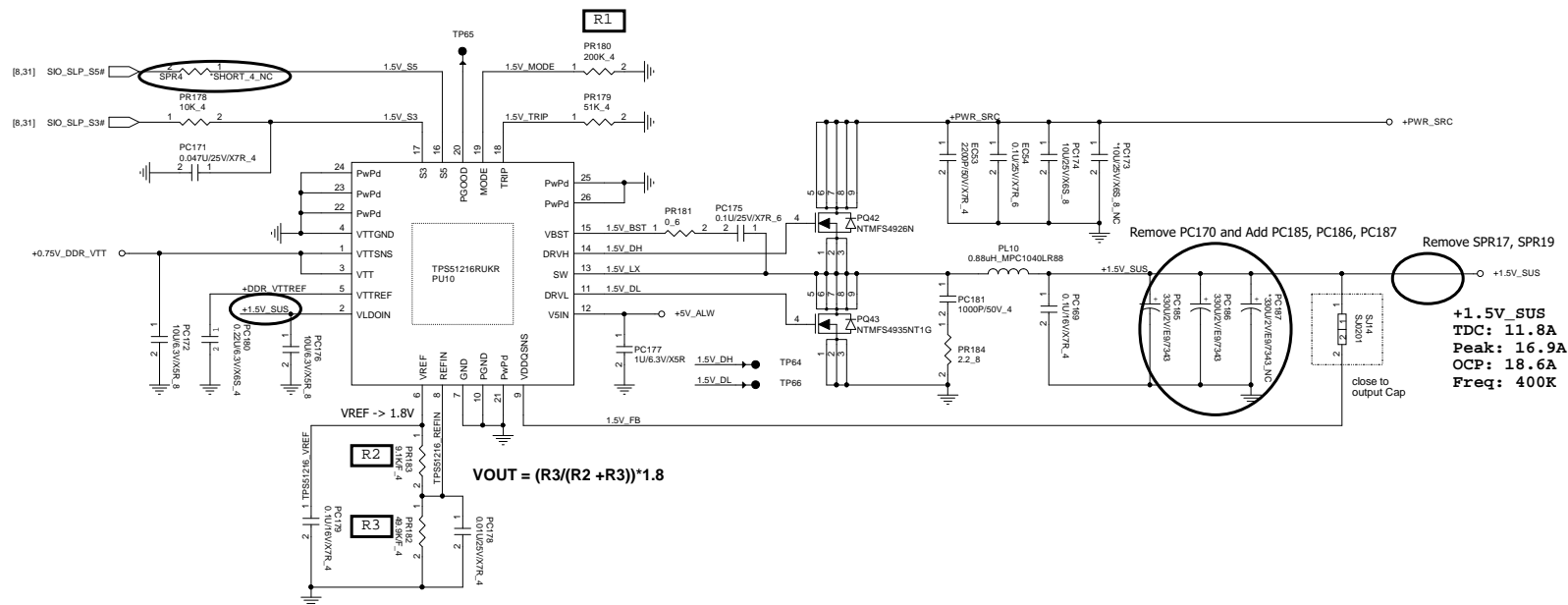
Date: Thursday, June 28, 2012 Sheet 38 of 55











Outputs Management by S3, S5 control

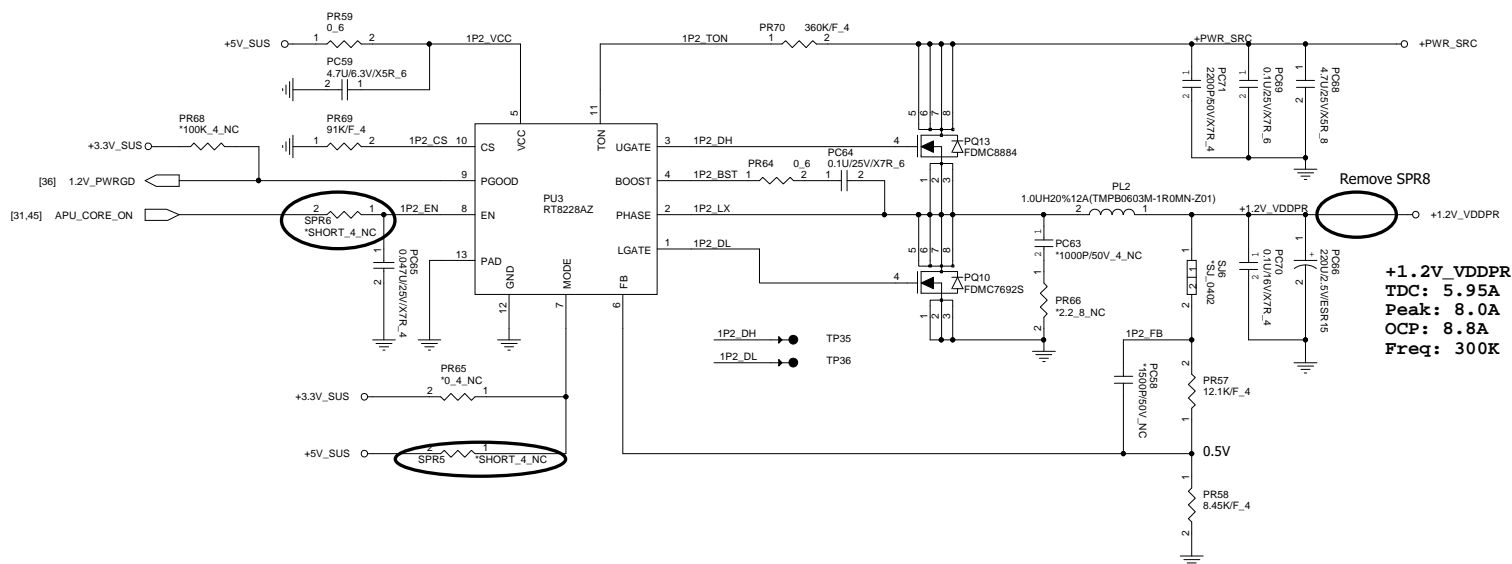
State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	Off (discharge)	Off (discharge)	Off (discharge)

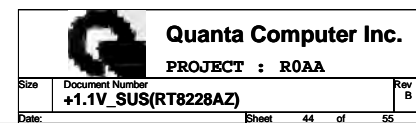
MODE Selection			
	Resistance between MODE and GND	Frequency	Discharge Mode
R1	200K_4	CS42002JB14	400k Hz
R1	100K_4	CS41002JB20	300k Hz
R1	68K_4	CS36802JB12	300k Hz
R1	47K_4	CS34702JB21	400k Hz

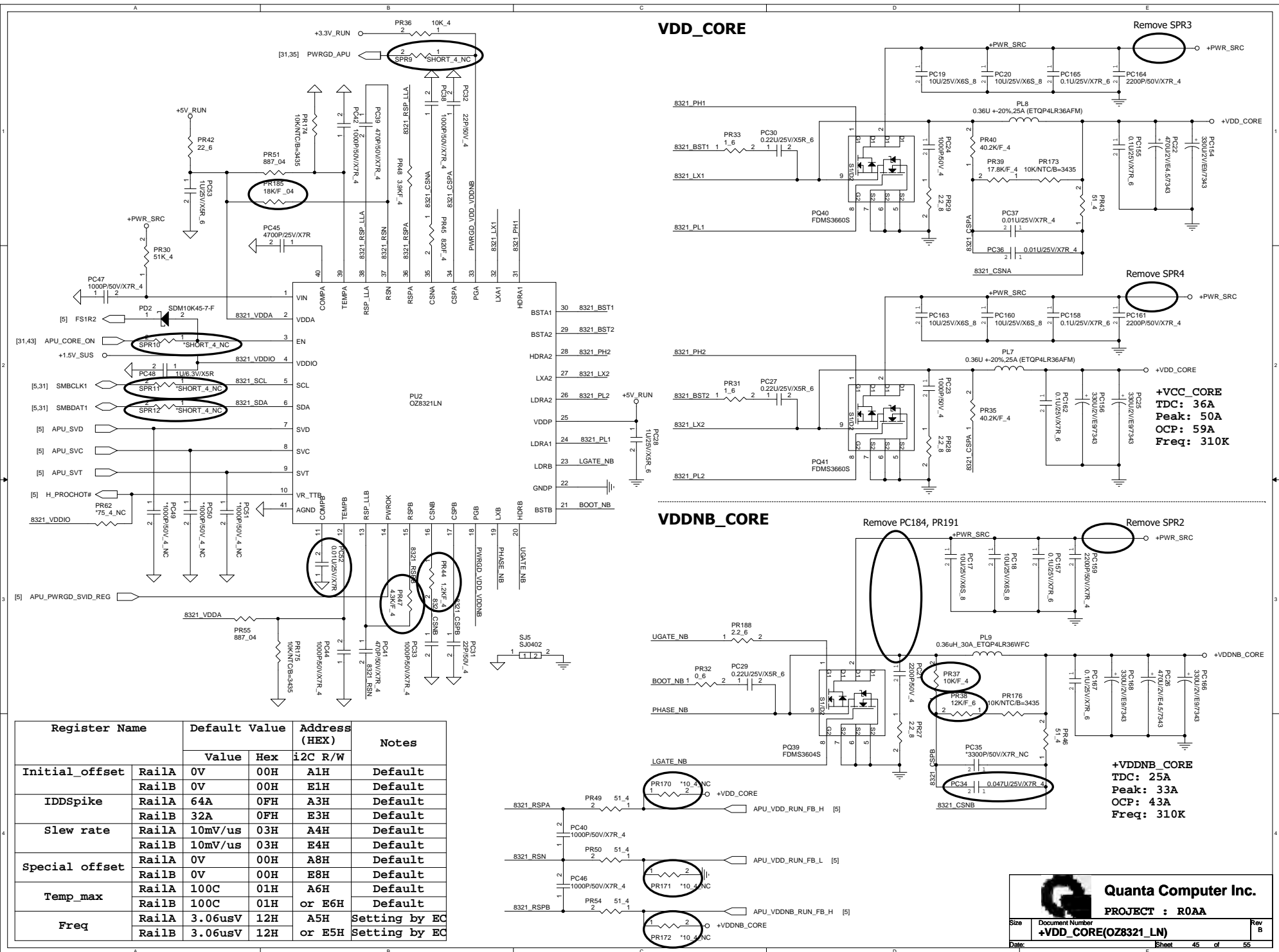
**Quanta Computer Inc.**  
 PROJECT : R0AA

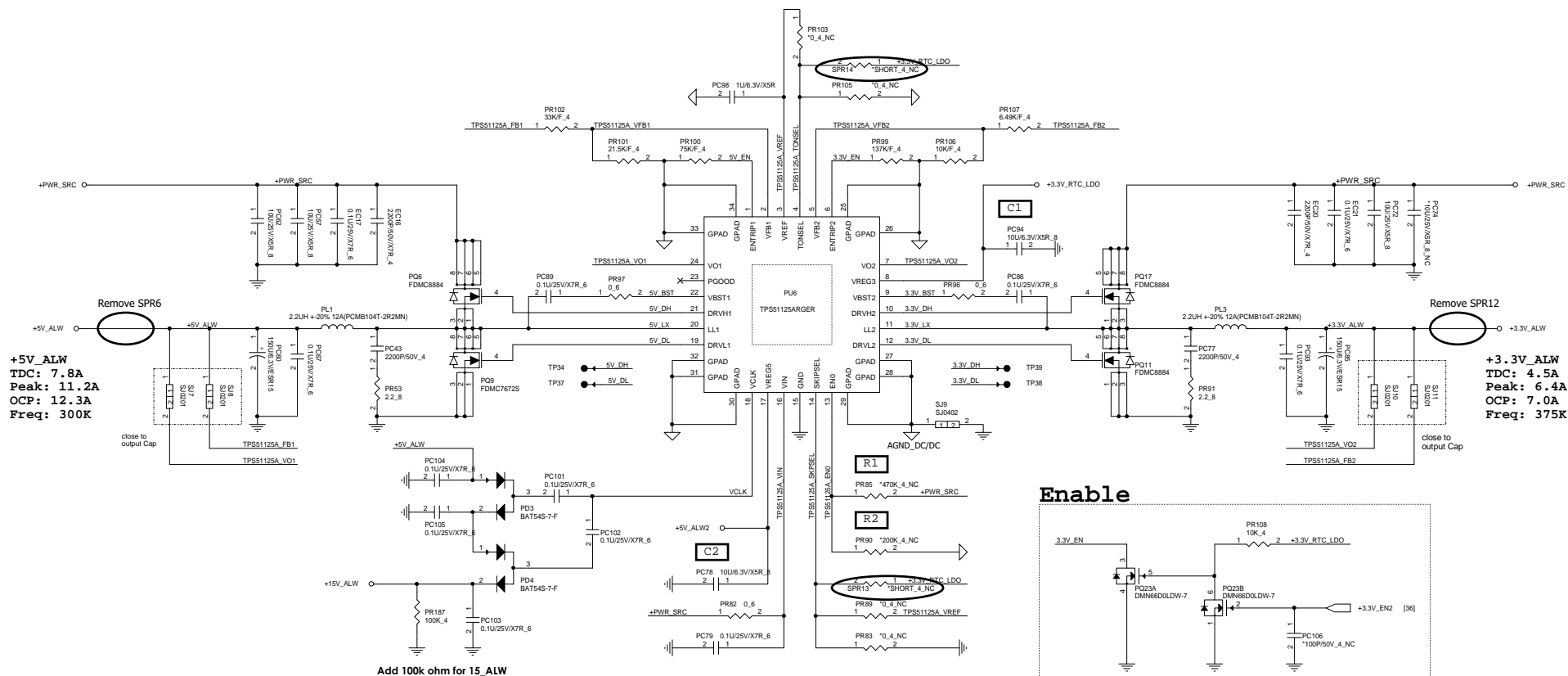
Size: Document Number: **+1.5V\_DDR/0.75V(TPS51216)** Rev B

Date: Sheet 42 of 55









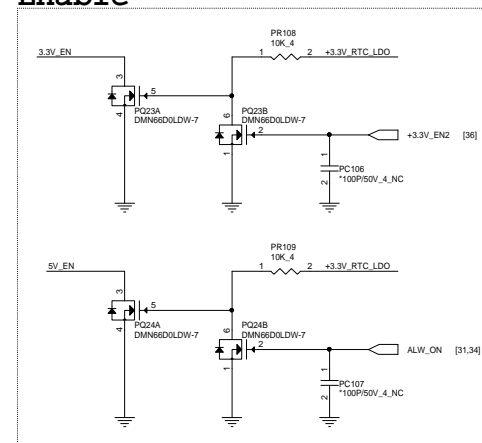
TPS51125A and RT8205N components differentia table

	TPS51125A	AL051125002	RT8205N	P/N not ready
R1	NC	N/A	R1 470K	CS44702JB15
R2	NC	N/A	R2 200K	CS42002JB14
R3	0_6	CS00003J951	R3 0_6	N/A
C1	10uF/6.3V_8	CH61001KA94	C1 4.7uF/6.3V_8	CH5471K1A00
C2	10uF/6.3V_8	CH61001KA94	C2 4.7uF/6.3V_8	CH5471K1A00
Q1	DDTA114YUA	N/A	Q1 DDTA114YUA	BA001140001
Q2	2N7002W-7-F	N/A	Q2 2N7002W-7-F	BAM70020040

TPS51125A TONSEL Connection and Switching Frequency

	REG5	REG3	VREF	GND
Channel1 Fs	365 kHz	300 kHz	245 kHz	200 kHz
Channel2 Fs	460 kHz	375 kHz	305 kHz	250 kHz

## Enable



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PROJECT : R0AA

Size Document Number  
+3.3V\_ALW / +5V\_ALW (TPS51125ARGER)  
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